CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
MAT 206	GRAPH THEORY	BSC	3	1	0	4

Preamble: This course introduces fundamental concepts in Graph Theory, including properties and characterisation of graph/trees and graph theoretic algorithms, which are widely used in Mathematical modelling and has got applications across Computer Science and other branches in Engineering.

Prerequisite: The topics covered under the course Discrete Mathematical Structures (MAT 203)

Course Outcomes: After the completion of the course the student will be able to

CO 1	Explain vertices and their properties, types of paths, classification of graphs and trees & their properties. **(Cognitive Knowledge Level: Understand)**
CO 2	Demonstrate the fundamental theorems on Eulerian and Hamiltonian graphs. **(Cognitive Knowledge Level: Understand)**
CO 3	Illustrate the working of Prim's and Kruskal's algorithms for finding minimum cost spanning tree and Dijkstra's and Floyd-Warshall algorithms for finding shortest paths. **(Cognitive Knowledge Level: Apply)**
CO 4	Explain planar graphs, their properties and an application for planar graphs. **(Cognitive Knowledge Level: Apply)**
CO 5	Illustrate how one can represent a graph in a computer. **(Cognitive Knowledge Level: Apply)**
CO 6	Explain the Vertex Color problem in graphs and illustrate an example application for vertex coloring. **(Cognitive Knowledge Level: Apply)**

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	√	√	√							√		√
CO 2	√	√	√	√						√		√
CO 3	√	√	√	√						√		√
CO 4	√	√	√	√						√		√
CO 5	√	√	√							√		√
CO 6	√	√	√			√				√		√

Abstract POs defined by National Board of Accreditation			
PO#	Broad PO	PO#	Broad PO
PO1	Engineering Knowledge	PO7	Environment and Sustainability
PO2	Problem Analysis	PO8	Ethics
PO3	Design/Development of solutions	PO9	Individual and team work
PO4	Conduct investigations of complex problems	PO10	Communication
PO5	Modern tool usage	PO11	Project Management and Finance
PO6	The Engineer and Society	PO12	Life long learning

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (%)		End Semester Examination (%)
	1	2	
Remember	30	30	30
Understand	30	30	30
Apply	40	40	40
Analyse			
Evaluate			
Create			

Mark Distribution

Total Marks	CIE Marks	ESE Marks	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance   : 10 marks

Continuous Assessment Tests   : 25 marks

Continuous Assessment Assignment : 15 marks

Internal Examination Pattern:

Each of the two internal examinations has to be conducted out of 50 marks

First Internal Examination shall be preferably conducted after completing the first half of the syllabus and the Second Internal Examination shall be preferably conducted after completing remaining part of the syllabus.

There will be two parts: Part A and Part B. Part A contains 5 questions (preferably, 2 questions each from the completed modules and 1 question from the partly covered module), having 3 marks for each question adding up to 15 marks for part A. Students should answer all questions from Part A. Part B contains 7 questions (preferably, 3 questions each from the completed modules and 1 question from the partly covered module), each with 7 marks. Out of the 7 questions in Part B, a student should answer any 5.

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer anyone. Each question can have maximum 2 sub-divisions and carries 14 marks.

Syllabus

Module 1

Introduction to Graphs : Introduction- Basic definition – Application of graphs – finite, infinite and bipartite graphs – Incidence and Degree – Isolated vertex, pendant vertex and Null graph. Paths and circuits – Isomorphism, sub graphs, walks, paths and circuits, connected graphs, disconnected graphs and components.

Module 2

Eulerian and Hamiltonian graphs : Euler graphs, Operations on graphs, Hamiltonian paths and circuits, Travelling salesman problem. Directed graphs – types of digraphs, Digraphs and binary relation, Directed paths, Fleury's algorithm.

Module 3

Trees and Graph Algorithms : Trees – properties, pendant vertex, Distance and centres in a tree - Rooted and binary trees, counting trees, spanning trees, Prim's algorithm and Kruskal's algorithm, Dijkstra's shortest path algorithm, Floyd-Warshall shortest path algorithm.

Module 4

Connectivity and Planar Graphs : Vertex Connectivity, Edge Connectivity, Cut set and Cut Vertices, Fundamental circuits, Planar graphs, Kuratowski's theorem (proof not required), Different representations of planar graphs, Euler's theorem, Geometric dual.

Module 5

Graph Representations and Vertex Colouring : Matrix representation of graphs-Adjacency matrix, Incidence Matrix, Circuit Matrix, Path Matrix. Coloring- Chromatic number, Chromatic polynomial, Matchings, Coverings, Four color problem and Five color problem. Greedy colouring algorithm.

Text book:

1. Narsingh Deo, Graph theory, PHI,1979

Reference Books:

1. R. Diestel, *Graph Theory,* free online edition, 2016: diestel-graph-theory.com/ basic.html.

2. Douglas B. West, Introduction to Graph Theory, Prentice Hall India Ltd.,2001

3. Robin J. Wilson, Introduction to Graph Theory, Longman Group Ltd.,2010

4. J.A. Bondy and U.S.R. Murty. Graph theory with Applications

Sample Course Level Assessment Questions.

Course Outcome 1 (CO1):

1. Differentiate a walk, path and circuit in a graph.

2. Is it possible to construct a graph with 12 vertices such that two of the vertices have degree 3 and the remaining vertices have degree 4? Justify

3. Prove that a simple graph with n vertices must be connected, if it has more than $\frac{(n-1)(n-2)}{2}$ edges.

4. Prove the statement: If a graph (connected or disconnected) has exactly two odd degree, then there must be a path joining these two vertices.

Course Outcome 2 (CO2):

1. Define Hamiltonian circuit and Euler graph. Give one example for each.

2. Define directed graphs. Differentiate between symmetric digraphs and asymmetric digraphs.

3. Prove that a connected graph G is an Euler graph if all vertices of G are of even degree.

4. Prove that a graph G of n vertices always has a Hamiltonian path if the sum of the degrees of every pair of vertices Vi, Vj in G satisfies the condition $d(Vi) + d(Vj) = n - 1$

Course Outcome 3 (CO3):

1. Discuss the centre of a tree with suitable example.

2. Define binary tree. Then prove that number of pendant vertices in a binary tree is $\frac{(n+1)}{2}$

3. Prove that a tree with n vertices has $n - 1$ edges.

4. Explain Floyd Warshall algorithm.

5. Run Dijkstra's algorithm on the following directed graph, starting at vertex S.
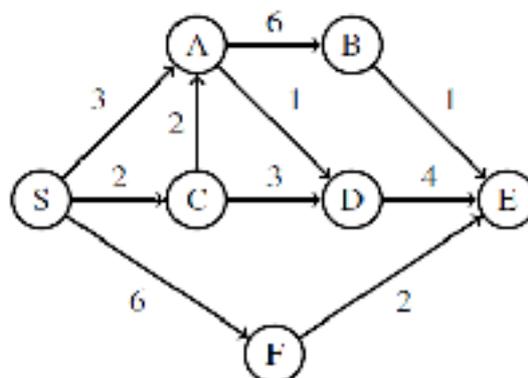
Course Outcome 4 (CO4):

1. Define edge connectivity, vertex connectivity and separable graphs. Give an example for each.

2. Prove that a connected graph with n vertices and e edges has $e - n + 2$ edges.

3. Prove the statement: Every cut set in a connected graph G must also contain at least one branch of every spanning tree of G.

4. Draw the geometrical dual *(G*)* of the graph given below, also check whether **G** and **G*** are self-duals or not, substantiate your answer clearly.
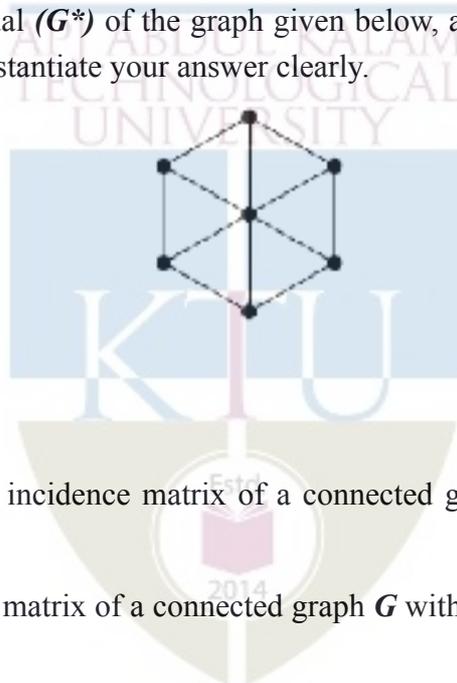
Course Outcome 5 (CO5):

1. Show that if *A(G)* is an incidence matrix of a connected graph *G* with *n* vertices, then rank of *A(G)* is *n−1*.

2. Show that if **B** is a cycle matrix of a connected graph *G* with *n* vertices and *m* edges, then rank **B** = *m−n+1*.

3. Derive the relations between the reduced incidence matrix, the fundamental cycle matrix, and the fundamental cut-set matrix of a graph *G*.

4. Characterize simple, self-dual graphs in terms of their cycle and cut-set matrices.

Course Outcome 6 (CO6):

1. Show that an n vertex graph is a tree iff its chromatic polynomial is $Pn(\lambda) = \lambda(\lambda - 1)^{n-1}$

2. Prove the statement: "A covering g of a graph is minimal if g contains no path of length three or more."

3. Find the chromatic polynomial of the graph

Model Question paper

QP
Code :

Total Pages: 4

Reg No.:_____   Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
IV SEMESTER B.TECH DEGREE EXAMINATION, MONTH and YEAR

Course Code: MAT 206

Course Name: GRAPH THEORY

Max. Marks: 100   Duration: 3 Hours

PART A

Answer all questions, each carries3 marks.   Marks

1   Construct a simple graph of 12 vertices with two of them having degree 1,   (3)
     three having degree 3 and the remaining seven having degree 10.

2   What is the largest number of vertices in a graph with 35 edges, if all   (3)
     vertices are of degree at least 3 ?

3   Define a Euler graph. Give an example of Eulerian graph which is not   (3)
     Hamiltonian

4   Give an example of a strongly connected simple digraph without a directed   (3)
     Hamiltonian path.

5   What is the sum of the degrees of any tree of *n* vertices?   (3)

6   How many spanning trees are there for the following graph   (3)
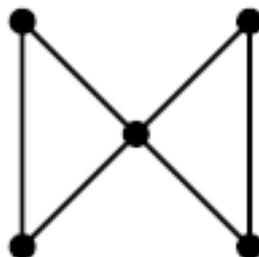
7   Show that in a simple connected planar graph G having V-vertices, E-edges,   (3)
     and no triangles $E \leq 3V - 6$.

8   Let G be the following disconnected planar graph. Draw its dual G*, and the   (3)
     dual of the dual (G*)*.

G
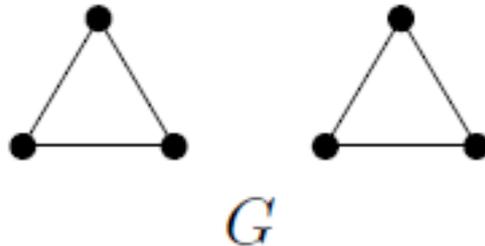
9   Consider the circuit matrix B and incidence matrix A of a simple connected   (3)
     graph whose columns are arranged using the same order of edges. Prove that
     every row of B is orthogonal to every row of A?

10   A graph is *critical* if the removal of any one of its vertices (and the edges   (3)
     adjacent to that vertex) results in a graph with a lower chromatic number.
   Show that K_n is critical for all $n > 1$.

PART B

Answer any one Question from each module. Each question carries 14 Marks

11 a) Prove that for any simple graph with at least two vertices has two vertices of   (6)
        the same degree.

    b) Prove that in a complete graph with n vertices there are $(n-1)/2$ edge disjoint   (8)
        Hamiltonian circuits and $n \geq 3$

OR

12 a) Determine whether the following graphs $G_1 = (V_1, E_1)$ and $G_2 = (V_2, E_2)$ are isomorphic or not. Give justification. (6)
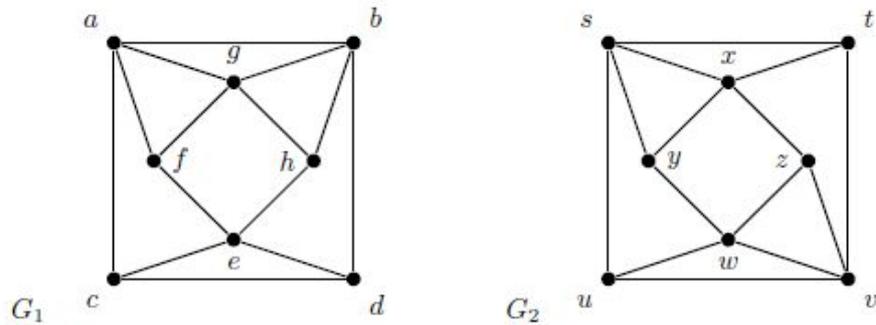

b) Prove that a simple graph with n vertices and k components can have at most $(n-k)(n-k+1)/2$ edges (8)

13 a) Let S be a set of 5 elements. Construct a graph G whose vertices are subsets of S of size 2 and two such subsets are adjacent in G if they are disjoint. (8)

    i. Draw the graph G.

    ii. How many edges must be added to G in order for G to have a Hamiltonian cycle?

b) Let G be a graph with exactly two connected components, both being Eulerian. What is the minimum number of edges that need to be added to G to obtain an Eulerian graph? (6)

OR

14 a) Show that a k-connected graph with no hamiltonian cycle has an independent set of size $k + 1$. (8)

b)   i. Let G be a graph that has exactly two connected components, both being Hamiltonian graphs. Find the minimum number of edges that one needs to add to G to obtain a Hamiltonian graph.

    ii. For which values of n the graph Q_n (hyper-cube on n vertices) is Eulerian. (6)

15 a) A tree T has at least one vertex v of degree 4, and at least one vertex w of degree 3. Prove that T has at least 5 leaves. (5)

b) Write Dijkstra's shortest path algorithm. (9)

Consider the following weighted directed graph **G**.
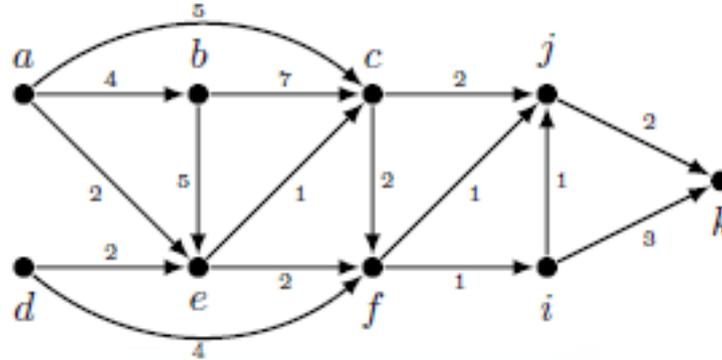
Find the shortest path between **a** and every other vertices in **G** using Dijkstra's shortest path algorithm.

OR

16 a) Define pendent vertices in a binary tree? Prove that the number of pendent (5) vertices in a binary tree with **n** vertices is **(n+1)/2.**

b) (9)
Write Prim's algorithm for finding minimum spanning tree.

Find a minimum spanning tree in the following weighted graph, using Prim's algorithm.
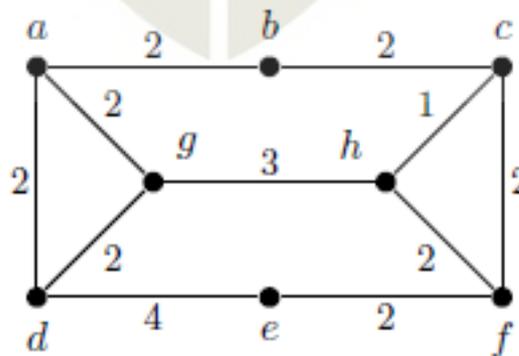
Determine the number of minimum spanning trees for the given graph.

17 a) i. State and prove Euler's Theorem relating the number of faces, edges and (9)
vertices for a planar graph.

   ii. If G is a 5-regular simple graph and $|V| = 10$, prove that G is non-planar.

b) Let G be a connected graph and e an edge of G. Show that e is a cut-edge if (5)
and only if e belongs to every spanning tree.

OR

18 a) State Kuratowski's theorem, and use it to show that the graph G below is not (9)
planar. Draw G on the plane without edges crossing. Your drawing should
use the labelling of the vertices given.
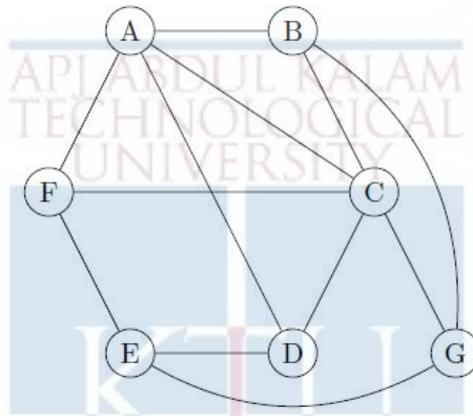
b) Let G be a connected graph and e an edge of G. Show that e belongs to a (5)
loop if and only if e belongs to no spanning tree.

19 a) Define the circuit matrix $B(G)$ of a connected graph G with n vertices and e (7)
edges with an example. Prove that the rank of $B(G)$ is $e-n+1$

b) Give the definition of the chromatic polynomial $P_G(k)$. Directly from the (7)
definition, prove that the chromatic polynomials of W_n and C_n satisfy the
identity $P_{Wn}(k) = k\ P_{Cn-1}\ (k-1)$.

OR

20 a) Define the incidence matrix of a graph G with an example. Prove that the (4)
rank of an incidence matrix of a connected graph with n vertices is $n-1$.

b) i. A graph G has chromatic polynomial $P_G(k) = k^4-4k^3+5k^2-2k$. How many vertices and edges does G have? Is G bipartite? Justify your answers.

ii. Find a maximum matching in the graph below and use Hall's theorem to show that it is indeed maximum.
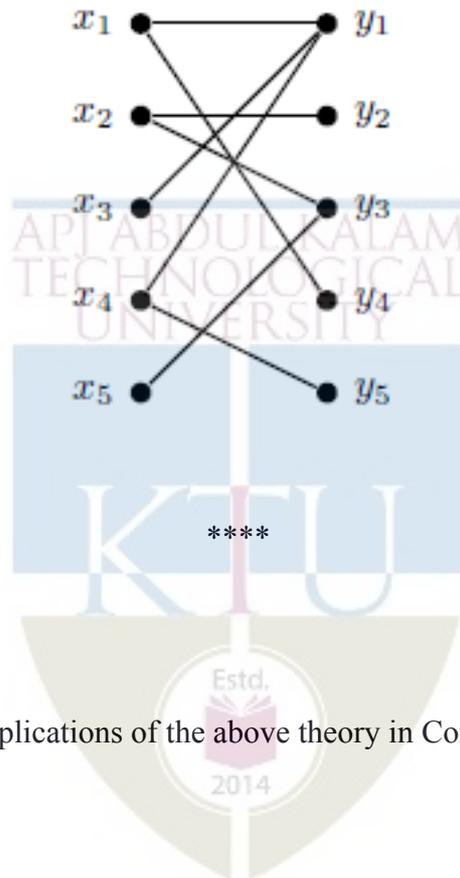
(10)

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Assignments

Assignment must include applications of the above theory in Computer Science.

	Teaching Plan	
No	Topic	No. of Lectures
1	**Module-I (Introduction to Graphs)**	**(8)**
1.	Introduction- Basic definition – Application of graphs – finite and infinite graphs, bipartite graphs,	1
2.	Incidence and Degree – Isolated vertex, pendent vertex and Null graph	1
3.	Paths and circuits	1
4.	Isomorphism	1
5.	Sub graphs, walks	1
6.	Paths and circuits	1
7.	Connected graphs.	1
8.	Disconnected graphs and components	1
2	**Module-II (Eulerian and Hamiltonian graphs)**	**(8)**
1.	Euler graphs	1
2.	Operations on graphs	1
3.	Hamiltonian paths and circuits	1
4.	Hamiltonian paths circuits	1
5.	Travelling salesman problem	1
6.	Directed graphs – types of digraphs,	1
7.	Digraphs and binary relation, Directed paths	1
8.	Fleury's algorithm	1
3	**Module-III (Trees and Graph Algorithms)**	**(11)**
1.	Trees – properties	1
2.	Trees – properties	1
3.	Trees – properties, pendent vertex	1
4.	Distance and centres in a tree	1

5.	Rooted and binary tree	1
6.	Counting trees	1
7.	Spanning trees, Fundamental circuits	1
8.	Prim's algorithm	1
9.	Kruskal's algorithm	1
10.	Dijkstra's shortest path algorithm	1
11.	Floyd-Warshall shortest path algorithm	1
4	**Module-IV (Connectivity and Planar Graphs)**	**(9)**
1.	Vertex Connectivity, Edge Connectivity	1
2.	Cut set and Cut Vertices	1
3.	Fundamental circuits	1
4.	Fundamental circuits	1
5.	Planar graphs	1
6.	Kuratowski's theorem	1
7.	Different representations of planar graphs	1
8.	Euler's theorem	1
9.	Geometric dual	1
5	**Module-V (Graph Representations and Vertex Colouring)**	**(9)**
1.	Matrix representation of graphs- Adjacency matrix, Incidence Matrix	1
2.	Circuit Matrix, Path Matrix	1
3.	Colouring- chromatic number,	1
4.	Chromatic polynomial	1
5.	Matching	1
6.	Covering	1
7.	Four colour problem and five colour problem	1

| 8. | Four colour problem and five colour problem | 1 |
| 9. | Greedy colouring algorithm. | 1 |
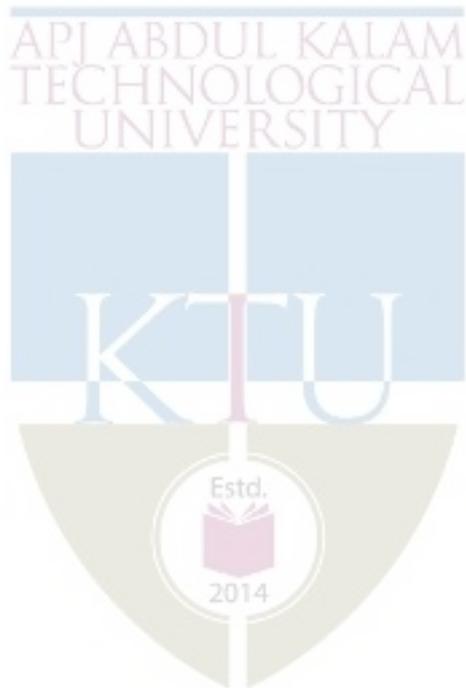
CST 202	Computer Organization and Architecture	CATEGORY	L	T	P	CREDIT	YEAR OF INTRODUCTION
		PCC	3	1	0	4	2019

Preamble:

The course is prepared with the view of enabling the learners capable of understanding the fundamental architecture of a digital computer. Study of Computer Organization and Architecture is essential to understand the hardware behind the code and its execution at physical level by interacting with existing memory and I/O structure. It helps the learners to understand the fundamentals about computer system design so that they can extend the features of computer organization to detect and solve problems occurring in computer architecture.

Prerequisite : Topics covered under the course Logic System Design (CST 203)

Course Outcomes: After the completion of the course the student will be able to

CO#	CO
CO1	Recognize and express the relevance of basic components, I/O organization and pipelining schemes in a digital computer **(Cognitive knowledge: Understand)**
CO2	Explain the types of memory systems and mapping functions used in memory systems **(Cognitive Knowledge Level: Understand)**
CO3	Demonstrate the control signals required for the execution of a given instruction **(Cognitive Knowledge Level: Apply))**
CO4	Illustrate the design of Arithmetic Logic Unit and explain the usage of registers in it **(Cognitive Knowledge Level: Apply)**
CO5	Explain the implementation aspects of arithmetic algorithms in a digital computer **(Cognitive Knowledge Level:Apply)**
CO6	Develop the control logic for a given arithmetic problem **(Cognitive Knowledge Level: Apply)**

Mapping of course outcomes with program outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓	✓	✓	✓								✓
CO2	✓	✓	✓	✓						✓		✓
CO3	✓	✓	✓	✓						✓		✓
CO4	✓	✓	✓	✓						✓		✓
CO5	✓	✓	✓							✓		✓
CO6	✓	✓	✓	✓								✓

Abstract POs defined by National Board of Accreditation			
PO#	**Broad PO**	**PO#**	**Broad PO**
PO1	Engineering Knowledge	PO7	Environment and Sustainability
PO2	Problem Analysis	PO8	Ethics
PO3	Design/Development of solutions	PO9	Individual and team work
PO4	Conduct investigations of complex problems	PO10	Communication
PO5	Modern tool usage	PO11	Project Management and Finance
PO6	The Engineer and Society	PO12	Life long learning

Assessment Pattern

Bloom's Category	Continuous Assessment Tests		End Semester Examination Marks (%)
	Test1 (%)	**Test2 (%)**	
Remember	20	20	30
Understand	40	40	30
Apply	40	40	40
Analyze			

Evaluate			
Create			

Mark Distribution

Total Marks	CIE Marks	ESE Marks	ESE Duration
150	50	100	3 hours

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Continuous Assessment Tests   : 25 marks

Continuous Assessment Assignment   : 15 marks

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There will be two parts: Part A and Part B. Part A contains 5 questions (preferably, 2 questions each from the completed modules and 1 question from the partly covered module), having 3 marks for each question adding up to 15 marks for part A. Students should answer all questions from Part A. Part B contains 7 questions (preferably, 3 questions each from the completed modules and 1 question from the partly covered module), each with 7 marks. Out of the 7 questions in Part B, a student should answer any 5.

End Semester Examination Pattern:

There will be two parts; Part A and Part B. Part A contains 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which a student should answer any one. Each question can have maximum 2 sub-divisions and carries 14 marks.

Syllabus

Module 1

Basic Structure of computers – functional units - basic operational concepts - bus structures. Memory locations and addresses - memory operations,Instructions and instruction sequencing , addressing modes.

Basic processing unit – fundamental concepts – instruction cycle – execution of a complete instruction - single bus and multiple bus organization

Module 2

Register transfer logic: inter register transfer – arithmetic, logic and shift micro operations.

Processor logic design: - processor organization – Arithmetic logic unit - design of arithmetic circuit - design of logic circuit - Design of arithmetic logic unit - status register – design of shifter - processor unit – design of accumulator.

Module 3

Arithmetic algorithms: Algorithms for multiplication and division (restoring method) of binary numbers. Array multiplier , Booth's multiplication algorithm.

Pipelining: Basic principles**,** classification of pipeline processors, instruction and arithmetic pipelines (Design examples not required), hazard detection and resolution.

Module 4

Control Logic Design: Control organization – Hard_wired control-microprogram control – control of processor unit - Microprogram sequencer,micro programmed CPU organization - horizontal and vertical micro instructions.

Module 5

I/O organization: accessing of I/O devices – interrupts, interrupt hardware -Direct memory access.

Memory system: basic concepts – semiconductor RAMs. memory system considerations – ROMs, Content addressable memory, cache memories - mapping functions.

Text Books

1. Hamacher C., Z. Vranesic and S. Zaky, Computer Organization ,5/e, McGraw Hill, 2011

2. Mano M. M., Digital Logic & Computer Design, PHI, 2004

3. KaiHwang, Faye Alye Briggs, Computer architecture and parallel processing McGraw-Hill, 1984

Reference Books

1. Mano M. M., Digital Logic & Computer Design, 3/e, Pearson Education, 2013.

2. Patterson D.A. and J. L. Hennessy, Computer Organization and Design, 5/e, Morgan Kaufmann Publishers, 2013.

3. William Stallings, Computer Organization and Architecture: Designing for Performance, Pearson, 9/e, 2013.

4. Chaudhuri P., Computer Organization and Design, 2/e, Prentice Hall, 2008.

5. Rajaraman V. and T. Radhakrishnan, Computer Organization and Architecture, Prentice Hall, 2011

Sample Course Level Assessment Questions

Course Outcome1(CO1): Which are the registers involved in a memory access operation and how are they involved in it?

Course Outcome 2(CO2): Explain the steps taken by the system to handle a write miss condition inside the cache memory.

Course Outcome 3(CO3): Generate the sequence of control signals required for the execution of the instruction MOV [R1],R2   in a threebus organization.

Course Outcome 4(CO4): Design a 4-bit combinational logic shifter with 2 control signals H0 and H1 that perform the following operations :

H1	H0	Operation
0	0	Transfer 1's to all output line
0	1	No shift operation
1	0	Shift left
1	1	Shift right

Course Outcome 5(CO5): Explain the restoring algorithm for binary division. Also trace the algorithm to divide $(1001)_2$ by $(11)_2$

Course Outcome 6(CO6): Design a software control logic based on microprogramed control to perform the addition of 2 signed numbers represented in sign magnitude form.
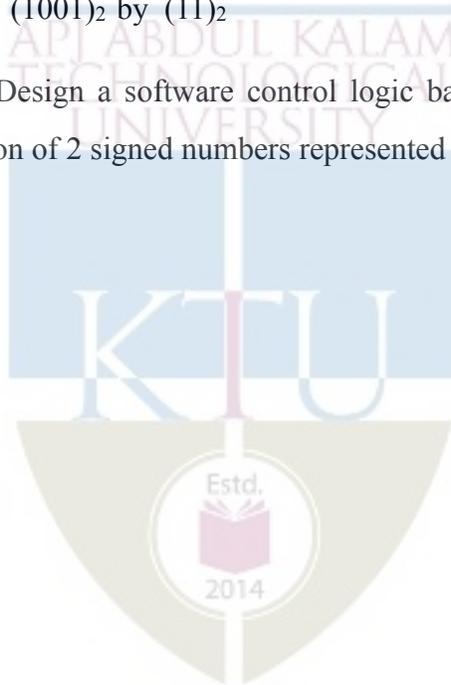
Model Question Paper

Reg No:_____

Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Code: CST 202

Course Name: Computer organization and architecture

Max.Marks:100   Duration: 3 Hours

PART A

Answer all Questions. Each question carries 3 Marks

1. Give the significance of instruction cycle.

2. Distinguish between big endian and little endian notations. Also give the significance of these notations.

3. Compare I/O mapped I/O and memory mapped I/O.

4. Give the importance of interrupts in I/O interconnection.

5. Justify the significance of status register.

6. How does the arithmetic circuitry perform logical operations in an ALU.

7. Illustrate divide overflow with an example.

8. Write notes on arithmetic pipeline.

9. Briefly explain the role of micro program sequence.

10. Differentiate between horizontal and vertical micro instructions.

Part B

Answer any one Question from each module. Each question carries 14 Marks

11.

    11.(a) What is the significance of addressing modes in computer architecture.

                (4)

    11.(b) Write the control sequence for the instruction DIV R1,[R2] in a three bus structure.
                (10)

OR

12. Explain the concept of a single bus organization with help of a diagram. Write the control sequence for the instruction ADD [R1],[R2].

                (14)

13. Explain various register transfer logics.

                (14)

OR

14.

    14.(a) Design a 4 bit combinational logic shifter with 2 control signals H1 and H2 that perform the following operations (bit values given in parenthesis are the values of control variable H1 and H2 respectively.) : Transfer of 0's to S (00), shift right (01), shift left (10), no shift (11).

                (5)

    14.(b) Design an ALU unit which will perform arithmetic and logic operation with a given binary adder.

                (9)

15.

    15.(a) Give the logic used behind Booth's multiplication algorithm.

                (4)

    15.(b) Identify the appropriate algorithm available inside the system   to perform the multiplication between -14 and -9. Also trace the algorithm for the above input.

                (10)

OR

16.

    16.(a) List and explain the different pipeline hazards and their possible solutions

                (10)

16.(b) Design a combinational circuit for 3x2 multiplication.

(4)

17. Design a hardwared control unit used to perform addition/subtraction of 2 numbers represented in sign magnitude form.

(14)

OR

18. Give the structure of the micro program sequencer and its role in sequencing the micro instructions.

(14)

19.

19.(a) Explain the different ways in which interrupt priority schemes can be implemented

(10)

19.(b) Give the structure of SRAM cell.

(4)

OR

20.

20.(a) Explain the various mapping functions available in cache memory.

(9)

20.(b) Briefly explain content addressable memory.

(5)

TEACHING PLAN

No	Contents	No of Lecture Hrs
Module 1 : (Basic Structure of computers) (9 hours)		
1.1	Functional units,basic operational concepts,bus structures (introduction)	1
1.2	Memory locations and addresses , memory operations	1
1.3	Instructions and instruction sequencing	1
1.4	Addressing modes	1
1.5	Fundamental concepts of instruction execution, instruction cycle	1
1.6	Execution of a complete instruction - single bus organization (Lecture 1)	1
1.7	Execution of a complete instruction - single bus organization (Lecture 2)	1
1.8	Execution of a complete instruction - multiple bus organization (Lecture 1)	1
1.9	Execution of a complete instruction - multiple bus organization (Lecture 2)	1
Module 2 :(Register transfer logic and Processor logic design) (10 hours)		
2.1	Inter register transfer – arithmetic micro operations	1
2.2	Inter register transfer – logic and shift micro operations	1
2.3	Processor organization	1
2.4	Design of arithmetic circuit	1
2.5	Design of logic circuit	1
2.6	Design of arithmetic logic unit	1
2.7	Design of status register	1
2.8	Design of shifter - processor unit	1

2.9	Design of accumulator (Lecture 1)	1
2.10	Design of accumulator (Lecture 2)	1
Module 3 : (Arithmetic algorithms and Pipelining) (9 hours)		
3.1	Algorithm for multiplication of binary numbers	1
3.2	Algorithm for division (restoring method) of binary numbers	1
3.3	Array multiplier	1
3.4	Booth's multiplication algorithm	1
3.5	Pipelining: Basic principles	1
3.6	Classification of pipeline processors (Lecture 1)	1
3.7	Classification of pipeline processors (Lecture 2)	1
3.8	Instruction and arithmetic pipelines (Design examples not required)	1
3.9	Hazard detection and resolution	1
Module 4 :(Control Logic Design) (9 hours)		
4.1	Control organization –design of hardwired control logic (Lecture 1)	1
4.2	Control organization –design of hardwired control logic (Lecture 2)	1
4.3	Control organization –design of hardwired control logic (Lecture 3)	1
4.4	Design of microprogram control logic–control of processor unit (Lecture1)	1
4.5	Design of microprogram control logic–control of processor unit (Lecture2)	1
4.6	Design of microprogram control logic–control of processor unit (Lecture3)	1
4.7	Microprogram sequencer	1
4.8	Micro programmed CPU organization	1
4.9	Microinstructions –horizontal and vertical micro instructions	1
Module 5 : (Basic processing units, I/O and memory) (8 hours)		
5.1	Accessing of I/O devices –interrupts	1
5.2	Interrupt hardware	1

5.3	Direct memory access	1
5.4	Memory system: basic concepts –semiconductor RAMs	1
5.5	Memory system considerations – ROMs	1
5.6	Content addressable memory	1
5.7	Cache memories -mapping functions (Lecture 1)	1
5.8	Cache memories -mapping functions (Lecture 2)	1
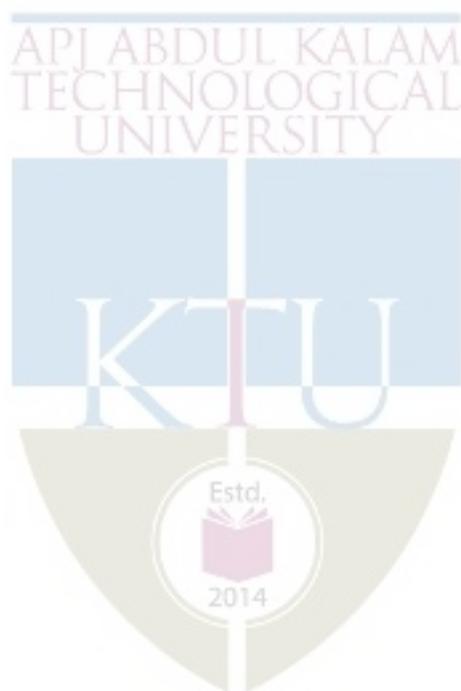
CST 204	Database Management Systems	CATEGORY	L	T	P	CREDIT	YEAR OF INTRODUCTION
		PCC	3	1	0	4	2019

Preamble: This course provides a clear understanding of fundamental principles of Database Management Systems (DBMS) with special focus on relational databases to the learners. The topics covered in this course are basic concepts of DBMS, Entity Relationship (ER) model, Relational Database principles, Relational Algebra, Structured Query Language (SQL), Physical Data Organization, Normalization and Transaction Processing Concepts. The course also gives a glimpse of the alternative data management model, NoSQL. This course helps the learners to manage data efficiently by identifying suitable structures to maintain data assets of organizations and to develop applications that utilize database technologies.

Prerequisite: Topics covered under the course Data Structures (CST 201), Exposure to a High Level Language like C/python.

Course Outcomes: After the completion of the course the student will be able to

CO1	Summarize and exemplify fundamental nature and characteristics of database systems **(Cognitive Knowledge Level: Understand)**
CO2	Model real word scenarios given as informal descriptions, using Entity Relationship diagrams. **(Cognitive Knowledge Level: Apply)**
CO3	Model and design solutions for efficiently representing and querying data using relational model **(Cognitive Knowledge Level: Analyze)**
CO4	Demonstrate the features of indexing and hashing in database applications **(Cognitive Knowledge Level: Apply)**
CO5	Discuss and compare the aspects of Concurrency Control and Recovery in Database systems **(Cognitive Knowledge Level: Apply)**
CO6	Explain various types of NoSQL databases **(Cognitive Knowledge Level: Understand)**

Mapping of course outcomes with program outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓	✓	✓									✓
CO2	✓	✓	✓	✓								✓
CO3	✓	✓	✓	✓								✓
CO4	✓	✓	✓							✓		✓
CO5	✓	✓	✓							✓		✓
CO6	✓	✓	✓		✓					✓		✓

Abstract POs defined by National Board of Accreditation			
PO#	**Broad PO**	**PO#**	**Broad PO**
PO1	Engineering Knowledge	PO7	Environment and Sustainability
PO2	Problem Analysis	PO8	Ethics
PO3	Design/Development of solutions	PO9	Individual and team work
PO4	Conduct investigations of complex problems	PO10	Communication
PO5	Modern tool usage	PO11	Project Management and Finance
PO6	The Engineer and Society	PO12	Life long learning

Assessment Pattern

Bloom's Category	Continuous Assessment Tests		End Semester Examination Marks (%)
	Test1 (%)	Test2 (%)	
Remember	30	30	30
Understand	40	40	40
Apply	30	30	30

Analyze			
Evaluate			
Create			

Mark Distribution

Total Marks	CIE Marks	ESE Marks	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance   : 10 marks

Continuous Assessment Tests   : 25 marks

Continuous Assessment Assignment   : 15 marks

Internal Examination Pattern:

Each of the two internal examinations has to be conducted out of 50 marks

First Internal Examination shall be preferably conducted after completing the first half of the syllabus and the Second Internal Examination shall be preferably conducted after completing remaining part of the syllabus.

There will be two parts: Part A and Part B. Part A contains 5 questions (preferably, 2 questions each from the completed modules and 1 question from the partly covered module), having 3 marks for each question adding up to 15 marks for part A. Students should answer all questions from Part A. Part B contains 7 questions (preferably, 3 questions each from the completed modules and 1 question from the partly covered module), each with 7 marks. Out of the 7 questions in Part B, a student should answer any 5.

End Semester Examination Pattern:

There will be two parts; Part A and Part B. Part A contains 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which a student should answer any one. Each question can have maximum 2 sub-divisions and carries 14 marks.

Syllabus

Module 1: Introduction & Entity Relationship (ER) Model

Concept & Overview of Database Management Systems (DBMS) - Characteristics of Database system, Database Users, structured, semi-structured and unstructured data. Data Models and Schema - Three Schema architecture. Database Languages, Database architectures and classification.

ER model **-** Basic concepts, entity set & attributes, notations, Relationships and constraints, cardinality, participation, notations, weak entities, relationships of degree 3.

Module 2: Relational Model

Structure of Relational Databases - Integrity Constraints, Synthesizing ER diagram to relational schema

Introduction to Relational Algebra - select, project, cartesian product operations, join - Equi-join, natural join. query examples, introduction to Structured Query Language (SQL), Data Definition Language (DDL), Table definitions and operations – CREATE, DROP, ALTER, INSERT, DELETE, UPDATE.

Module 3: SQL DML (Data Manipulation Language), Physical Data Organization

SQL DML (Data Manipulation Language) - SQL queries on single and multiple tables, Nested queries (correlated and non-correlated), Aggregation and grouping, Views, assertions, Triggers, SQL data types.

Physical Data Organization - Review of terms: physical and logical records, blocking factor, pinned and unpinned organization. Heap files, Indexing, Singe level indices, numerical examples, Multi-level-indices, numerical examples, B-Trees & B+-Trees (structure only, algorithms not required), Extendible Hashing, Indexing on multiple keys – grid files.

Module 4: Normalization

Different anomalies in designing a database, The idea of normalization, Functional dependency, Armstrong's Axioms (proofs not required), Closures and their computation, Equivalence of Functional Dependencies (FD), Minimal Cover (proofs not required). First Normal Form (1NF), Second Normal Form (2NF), Third Normal Form (3NF), Boyce Codd Normal Form (BCNF), Lossless join and dependency preserving decomposition, Algorithms for checking Lossless Join (LJ) and Dependency Preserving (DP) properties.

Module 5: Transactions, Concurrency and Recovery, Recent Topics

Transaction Processing Concepts - overview of concurrency control, Transaction Model, Significance of concurrency Control & Recovery, Transaction States, System Log, Desirable Properties of transactions.
Serial schedules, Concurrent and Serializable Schedules, Conflict equivalence and conflict serializability, Recoverable and cascade-less schedules, Locking, Two-phase locking and its variations. Log-based recovery, Deferred database modification, check-pointing.

Introduction to NoSQL Databases, Main characteristics of Key-value DB (examples from: Redis), Document DB (examples from: MongoDB)

Main characteristics of Column - Family DB (examples from: Cassandra) and Graph DB (examples from : ArangoDB)

Text Books

1. Elmasri R. and S. Navathe, Database Systems: Models, Languages, Design and Application Programming, Pearson Education, 2013.

2. Sliberschatz A., H. F. Korth and S. Sudarshan, Database System Concepts, 6/e, McGraw Hill, 2011.

Reference Books:
1. Adam Fowler, NoSQL for Dummies, John Wiley & Sons, 2015
2. NoSQL Data Models: Trends and Challenges (Computer Engineering: Databases and Big Data), Wiley, 2018
3. Web Resource: https://www.w3resource.com/redis/
4. web Resource: https://www.w3schools.in/category/mongodb/
5. Web Resource: https://www.tutorialspoint.com/cassandra/cassandra_introduction.htm
6. Web Resource : https://www.tutorialspoint.com/arangodb/index.htm

Sample Course Level Assessment Questions

Course Outcome1 (CO1):

1. List out any three salient features of database systems, which distinguish it from a file system.
2. Give one example each for logical and physical data independence.

Course Outcome 2(CO2):

1. What facts about the relationships between entities EMPLOYEE and PROJECT are conveyed by the following ER diagram?

1. Design an ER diagram for the following scenario:
   There is a set of teams, each team has an ID (unique identifier), name, main stadium, and to which city this team belongs. Each team has many players, and each player belongs to one team. Each player has a number (unique identifier), name, DoB, start year, and shirt number that he uses. Teams play matches, in each match there is a host team and a guest team.

Course Outcome 3(CO3):

1. For the SQL query, SELECT *A, B FROM R WHERE B='apple' AND C = 'orange'* on the table R(A, B, C, D), where A is a key, write any three equivalent relational algebra expressions.
2. Given the FDs P→Q, P→R, QR→S, Q→T, QR→U, PR→U, write the sequence of *Armstrong's Axioms* needed to arrive at the following FDs: (a) P → T (b) PR → S (c) QR → SU
3. Consider a relation PLAYER (PLAYER-NO, PLAYER-NAME, PLAYER-POSN, TEAM, TEAM-COLOR, COACH-NO, COACH-NAME, TEAM-CAPTAIN). Assume that PLAYER-NO is the *only* key of the relation and that the following dependencies hold:
   TEAM→{TEAM-COLOR, COACH-NO, TEAM-CAPTAIN}
   COACH-NO→COACH-NAME.
   i.   Is the relation in 2NF? If not, decompose to 2NF.
   ii. Is the relation in 3NF? If not, decompose to 3NF.

4. In the following tables foreign keys have the same name as primary keys except DIRECTED-BY, which refers to the primary key ARTIST-ID. Consider only *single-director* movies.

    MOVIES(<u>MOVIE-ID</u>, MNAME, GENRE, LENGTH, DIRECTED-BY)
    ARTIST(<u>ARTIST-ID</u>, ANAME)
    ACTING(<u>ARTIST-ID, MOVIE-ID</u>)

    Write SQL expressions for the following queries:
    (a) Name(s) and director name(s) of movie(s) acted by 'Jenny'.
    (b) Names of actors who have <u>never</u> acted with 'Rony'
    (c) Count of movies genre-wise.
    (d) Name(s) of movies with maximum length.

Course Outcome 4(CO4):

1. Consider an EMPLOYEE file with 10000 records where each record is of size 80 bytes. The file is sorted on employee number (15 bytes long), which is the primary key. Assuming un-spanned organization, block size of 512 bytes and block pointer size of 5 bytes. Compute the number of block accesses needed for retrieving an employee record based on employee number if (i) No index is used (ii) Multi-level primary index is used.

Course Outcome 5(CO5):

1. Determine if the following schedule is *recoverable*. Is the schedule *cascade-less*? Justify your answer. $r1(X), r2(Z), r1(Z), r3(X), r3(Y), w1(X), c1, w3(Y), c3, r2(Y), w2(Z), w2(Y), c2$. (*Note: $ri(X)/wi(X)$* means transaction *Ti* issues read/write on item X; *ci* means transaction *Ti* commits.)
2. Two-phase locking protocol ensures serializability. Justify.

Course Outcome 6(CO6):

1. List out any three salient features of NoSQL databases. Give example of a document in MongoDB.

Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Code: CST 204

Course Name: **Database Management Systems**

Max.Marks:100   **Duration: 3 Hours**

PART A

Answer all Questions. Each question carries 3 Marks

1 List out any three salient features of a database systems.

2 When is multi-valued composite attribute used in ER modelling?

3 For the SQL query, SELECT *A, B FROM R WHERE B='apple' AND C = 'orange'* on the table R(A, B, C, D), where A is a key, write any two equivalent relational algebra expressions.

4 Outline the concept of *theta*-join.

5 How is the purpose of *where* clause is different from that of having clause?

6 What is the use of a trigger?

7 When do you say that a relation is not in 1NF?

8 Given the FDs P→Q, P→R, QR→S, Q→T, QR→U, PR→U, write the sequence of Armstrong's Axioms needed to arrive at a. P → T   b. PR → S

9 What is meant by the lost update problem?

10 What is meant by check pointing?

PART B

Answer any one Question from each module. Each question carries 14 Marks

11 a. Design an ER diagram for the following scenario: There is a set of teams, each (14)
        team has an ID (unique identifier), name, main stadium, and to which city this
        team belongs. Each team has many players, and each player belongs to one
        team. Each player has a number (unique identifier), name, DoB, start year, and
        shirt number that he uses. Teams play matches, in each match there is a host
        team and a guest team. The match takes place in the stadium of the host team.
        For each match we need to keep track of the following: The date on which the
        game is played The final result of the match. The players participated in the
        match. For each player, how many goals he scored, whether or not he took
        yellow card, and whether or not he took red card. During the match, one player
        may substitute another player. We want to capture this substitution and the time
        at which it took place. Each match has exactly three referees. For each referee
        we have an ID (unique identifier), name, DoB, years of experience. One referee
        is the main referee and the other two are assistant referee.

OR

12 a. Interpret the the following ER diagram.

(8)
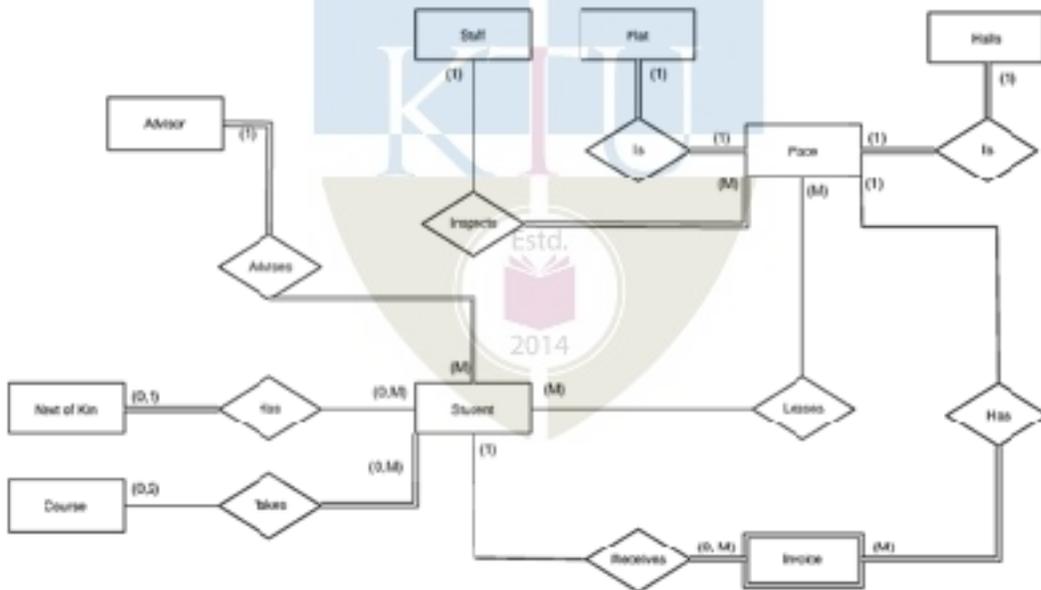
    b. Distinguish between physical data independence and logical data independence (6)
        with suitable examples.

13 **EMPLOYEE(ENO, NAME, ADDRESS, DOB, AGE, GENDER, SALARY, DNUM, SUPERENO)**
DEPARTMENT(DNO, DNAME, DLOCATION, DPHONE, MGRENO)
PROJECT(PNO, PNAME, PLOCATION, PCOST, CDNO)   (14)

DNUM is a foreign key that identifies the department to which an employee belongs. MGRENO is a foreign key identifying the employee who manages the department. CDNO is a foreign key identifying the department that controls the project. SUPERENO is a foreign key identifying the supervisor of each employee.

Write relational algebra expressions for the following queries:-

(a) Names of female employees whose salary is more than 20000.
(b) Salaries of employee from 'Accounts' department
(c) Names of employees along with his/her superviser's name
(d) For each employee return name of the employee along with his department name and the names of projects in which he/she works
(e) Names of employees working in all the departments

OR

14   a. Write SQL DDL statements for the the following (Assume suitable domain types):   (10)

  i.   Create the tables STUDENT(ROLLNO, NAME, CLASS, SEM, ADVISER), FACULTY(FID, NAME, SALARY, DEPT). Assume that ADVISER is a foreign key referring FACUTY table.

  ii.   Delete department with name 'CS' and all employees of the department.

  iii. Increment salary of every faculty by 10%.

  b. Illustrate foreign key constraint with a typical example.   (4)

15 For the relation schema below, give an expression in SQL for each of the queries (14) that follows:

employee(**employee-name**, street, city)
works(**employee-name, company-name**, salary)
company(**company-name**, city)
manages(**employee-name, manager-name**)

a) Find the names, street address, and cities of residence for all employees who work for the Company 'RIL Inc.' and earn more than $10,000.
b) Find the names of all employees who live in the same cities as the companies for which they work.
c) Find the names of all employees who do not work for 'KYS Inc.'. Assume that all people work for exactly one company.
d) Find the names of all employees who earn more than every employee of 'SB Corporation'. Assume that all people work for at most one company.
e) List out number of employees company-wise in the decreasing order of number of employees.

OR

16 a. Consider an EMPLOYEE file with 10000 records where each record is of (9) size 80 bytes. The file is sorted on employee number (15 bytes long), which is the primary key. Assuming un-spanned organization and block size of 512 bytes compute the number of block accesses needed for selecting records based on employee number if,
   i.   No index is used
   ii.   Single level primary index is used
   iii.   Multi-level primary index is used
   Assume a block pointer size of 6 bytes.

b. Illustrate correlated and non-correlated nested queries with real examples. (5)

17 a. Illstrate3NF and BCNF with suitable real examples. (6)

b. Given a relation R(A1,A2,A3,A4,A5) with functional dependencies (8) A1→A2A4 and A4→A5, check if the decomposition R1(A1,A2,A3), R2(A1,A4), R3(A2,A4,A5) is lossless.

OR

18 a. Consider the un-normalized relation R(A, B, C, D, E, F, G) with the FDs (7) A→B , AC→G, AD→EF, EF→G, CDE→AB. Trace the normalization process to reach 3NF relations.

b. Illustrate Lossless Join Decomposition and Dependency Preserving Decomposition with typical examples. (7)

19 a. Discuss the four ACID properties and their importance. (7)

b. Determine if the following schedule is conflict serializable. Is the schedule recoverable? Is the schedule cascade-less? Justify your answers. (7)

r1(X), r2(Z), r1(Z), r3(X), r3(Y), w1(X), c1, w3(Y), c3, r2(Y), w2(Z), w2(Y), c2

(Note: ri(X)/wi(X) means transaction Ti issues read/write on item X; ci means transaction Ti commits.)

OR

20 a. Discuss the main characteristics of Key-value DB and Graph DB. (7)

b. Illustrate two-phase locking with a schedule containing three transactions. Argue that 2PL ensures serializability. Also argue that 2Pl can lead to deadlock. (7)
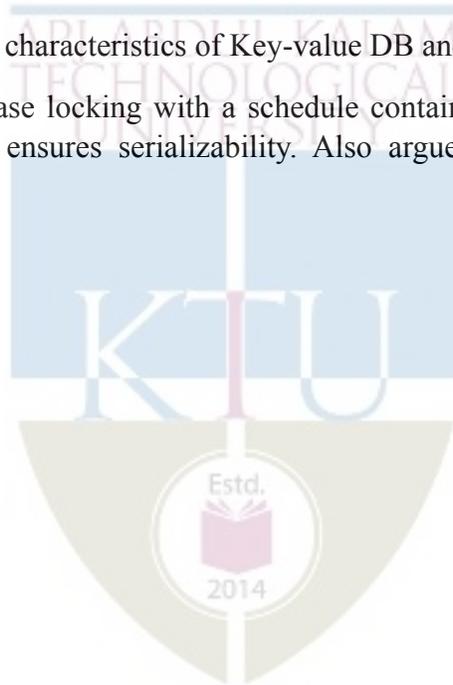
Teaching Plan

	Course Name	Hours (48)
	Module 1: Introduction & ER Model	**8**
1.1	Concept & Overview of DBMS, Characteristics of DB system, Database Users.	1
1.2	Structured, semi-structured and unstructured data. Data Models and Schema	1
1.3	Three-Schema-architecture. Database Languages	1
1.4	Database architectures and classification	1
1.5	ER model: basic concepts, entity set & attributes, notations	1
1.6	Relationships and constraints – cardinality, participation, notations	1
1.7	Weak entities, relationships of degree 3	1
1.8	ER diagram – exercises	1
	Module 2: Relational Model	**7**
2.1	Structure of relational Databases, Integrity Constraints	1
2.2	Synthesizing ER diagram to relational schema, Introduction to relational algebra.	1
2.3	Relational algebra: select, project, Cartesian product operations	1
2.4	Relational Algebra: join - Equi-join, Natural join	1
2.5	Query examples	1
2.6	Introduction to SQL, important data types	1
2.7	DDL, Table definitions and operations – CREATE, DROP, ALTER, INSERT, DELETE, UPDATE	1
	Module 3: SQL DML, Physical Data Organization	**11**
3.1	SQL DML, SQL queries on single and multiple tables	1
3.2	Nested queries (correlated and non-correlated)	1
3.3	Aggregation and grouping	1

	Course Name	**Hours (48)**
3.4	Views, assertions (with examples)	1
3.5	Triggers (with examples), SQL data types	1
3.6	Review of terms: physical and logical records, blocking factor, pinned and unpinned organization. Heap files, Indexing	1
3.7	Singe level indices, numerical examples	1
3.8	Multi-level-indices, numerical examples	1
3.9	B-Trees and B+Trees (structure only, algorithms not required)	1
3.10	Extendible Hashing	1
3.11	Indexing on multiple keys – grid files	1
	Module 4: Normalization	**8**
4.1	Different anomalies in designing a database, The idea of normalization	1
4.2	Functional dependency, Armstrong's Axioms (proofs not required)	1
4.3	Closures and their computation, Equivalence of FDs, minimal Cover (proofs not required).	1
4.4	1NF, 2NF	1
4.5	3NF, BCNF	1
4.6	Lossless join and dependency preserving decomposition	1
4.7	Algorithms for checking Lossless Join and Dependency preserving properties (Lecture 1)	1
4.8	Algorithms for checking Lossless Join and Dependency preserving properties (Lecture 2)	1
	Module 5: Transactions, Concurrency and Recovery, Recent Topics	**14**
5.1	Transaction Processing Concepts: Transaction Model	1
5.2	Overview of concurrency control, Significance of concurrency Control & Recovery	1
5.3	Transaction States, System Log	1

	Course Name	Hours (48)
5.4	Desirable Properties of transactions, Serial schedules	1
5.5	Concurrent and Serializable Schedules	1
5.6	Conflict equivalence and conflict serializability	1
5.7	Recoverable and cascade-less schedules	1
5.8	Locking, Two-phase locking, strict 2PL.	1
5.9	Log-based recovery	1
5.10	Deferred database modification (serial schedule), example	1
5.11	Deferred database modification (concurrent schedule) example, check-pointing	1
5.12	Introduction to NoSQL Databases	1
5.13	Main characteristics of Key-value DB (examples from: Redis), Document DB (examples from: MongoDB) [detailed study not expected]	1
5.14	Main characteristics of Column-Family DB (examples from: Cassandra) and Graph DB (examples from : ArangoDB) [detailed study not expected]	1

CST 206	OPERATING SYSTEMS	Category	L	T	P	Credit	Year of Introduction
		PCC	3	1	0	4	2019

Preamble: Study of operating system is an essential to understand the overall working of computer system, tradeoffs between performance and functionality and the division of jobs between hardware and software. This course introduces the concepts of memory management, device management, process management, file management and security & protection mechanisms available in an operating system. The course helps the learner to understand the fundamentals about any operating system design so that they can extend the features of operating system to detect and solve many problems occurring in operating system and to manage the computer resources appropriately.

Prerequisite: Topics covered in the courses are **Data Structures (CST 201)** and **Programming in C (EST 102)**

Course Outcomes: After the completion of the course the student will be able to

CO1	Explain the relevance, structure and functions of Operating Systems in computing devices. (**Cognitive knowledge: Understand**)
CO2	Illustrate the concepts of process management and process scheduling mechanisms employed in Operating Systems. (**Cognitive knowledge: Understand**)
CO3	Explain process synchronization in Operating Systems and illustrate process synchronization mechanisms using Mutex Locks, Semaphores and Monitors (**Cognitive knowledge: Understand**)
CO4	Explain any one method for detection, prevention, avoidance and recovery for managing deadlocks in Operating Systems. (**Cognitive knowledge: Understand**)
CO5	Explain the memory management algorithms in Operating Systems. (**Cognitive knowledge: Understand**)
CO6	Explain the security aspects and algorithms for file and storage management in Operating Systems. (**Cognitive knowledge: Understand**)

Mapping of course outcomes with program outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓	✓	✓							✓		✓
CO2	✓	✓	✓	✓						✓		✓
CO3	✓	✓	✓	✓						✓		✓
CO4	✓	✓	✓	✓						✓		✓
CO5	✓	✓	✓	✓						✓		✓
CO6	✓	✓	✓	✓						✓		✓

Abstract POs defined by National Board of Accreditation			
PO#	Broad PO	PO#	Broad PO
PO1	Engineering Knowledge	PO7	Environment and Sustainability
PO2	Problem Analysis	PO8	Ethics
PO3	Design/Development of solutions	PO9	Individual and team work
PO4	Conduct investigations of complex problems	PO10	Communication
PO5	Modern tool usage	PO11	Project Management and Finance
PO6	The Engineer and Society	PO12	Life long learning

Assessment Pattern

Bloom's Category	Test 1 (Marks in percentage)	Test 2 (Marks in percentage)	End Semester Examination (Marks in percentage)
Remember	30	30	30
Understand	30	30	30
Apply	40	40	40
Analyse			
Evaluate			
Create			

Mark Distribution

Total Marks	CIE Marks	ESE Marks	ESE Duration
150	50	100	3

Continuous Internal Evaluation Pattern:
Attendance   : 10 marks
Continuous Assessment Test   : 25 marks
Continuous Assessment Assignment : 15 marks

Internal Examination Pattern:

Each of the two internal examinations has to be conducted out of 50 marks. First series test shall be preferably conducted after completing the first half of the syllabus and the second series test shall be preferably conducted after completing remaining part of the syllabus. There will be two parts: Part A and Part B. Part A contains 5 questions (preferably, 2 questions each from the completed modules and 1 question from the partly completed module), having 3 marks for each question adding up to 15 marks for part A. Students should answer all questions from Part A. Part B contains 7 questions (preferably, 3 questions each from the completed modules and 1 question from the partly completed module), each with 7 marks. Out of the 7 questions, a student should answer any 5.

End Semester Examination Pattern:
There will be two parts; Part A and Part B. Part A contains 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which a student should answer any one. Each question can have maximum 2 sub-divisions and carries 14 marks.

Syllabus

Module I

Introduction: Operating system overview – Operations, Functions, Service – System calls, Types – Operating System structure - Simple structure, Layered approach, Microkernel, Modules – System boot process.

Module II

Processes - Process states, Process control block, threads, scheduling, Operations on processes - process creation and termination – Inter-process communication - shared memory systems, Message passing systems.

Process Scheduling – Basic concepts- Scheduling criteria -scheduling algorithms- First come First Served, Shortest Job Firs, Priority scheduling, Round robin scheduling

Module III

Process synchronization- Race conditions –   Critical section problem – Peterson's solution, Synchronization hardware, Mutex Locks, Semaphores, Monitors – Synchronization problems - Producer Consumer, Dining Philosophers and Readers-Writers.

Deadlocks: Necessary conditions, Resource allocation graphs, Deadlock prevention, Deadlock avoidance – Banker's algorithms, Deadlock detection, Recovery from deadlock.

Module IV

Memory Management: Concept of address spaces, Swapping, Contiguous memory allocation, fixed and variable partitions, Segmentation,   Paging. Virtual memory,   Demand paging, Page replacement algorithms.

Module V

File System: File concept - Attributes, Operations, types, structure – Access methods, Protection. File-system implementation, Directory implementation. Allocation methods.
Storage Management: Magnetic disks, Solid-state disks, Disk Structure, Disk scheduling, Disk formatting.

Text Book

Abraham Silberschatz, Peter Baer Galvin, Greg Gagne, ' Operating   System Concepts' 9th Edition, Wiley India 2015.

Reference Books:

1. Andrew S Tanenbaum, "Modern Operating Systems" , 4th Edition, Prentice Hall, 2015.
2. William Stallings, "Operating systems", 6th Edition, Pearson, Global Edition, 2015.
3. Garry Nutt, Nabendu Chaki, Sarmistha Neogy, "Operating Systems", 3rd Edition, Pearson Education.
4. D.M.Dhamdhere, "Operating Systems", 2nd Edition, Tata McGraw Hill, 2011.
5. Sibsankar Haldar, Alex A Aravind, "Operating Systems", Pearson Education.

Sample Course Level Assessment Questions

Course Outcome1 (CO1): What is the main advantage of the micro kernel approach to system design? How do user program and system program interact in a microkernel architecture?

Course Outcome 2 (CO2): Define process. With the help of a neat diagram explain different states of process.

Course Outcome 3 (CO3): What do you mean by binary semaphore and counting semaphore? With C, explain implementation of wait () and signal().

Course Outcome 4 (CO4): Describe resource allocation graph for the following. a) with a deadlock   b) with a cycle but no deadlock.

Course Outcome 5 (CO5): Consider the following page reference string 1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 2, 3, 7, 6, 3, 2, 1, 2, 3, 6. Find out the number of page faults if there are 4 page frames, using the following page replacement algorithms. i) LRU ii) FIFO iii) Optimal

Course Outcome 6 (CO6): Explain the different file allocation methods with advantages and disadvantages.
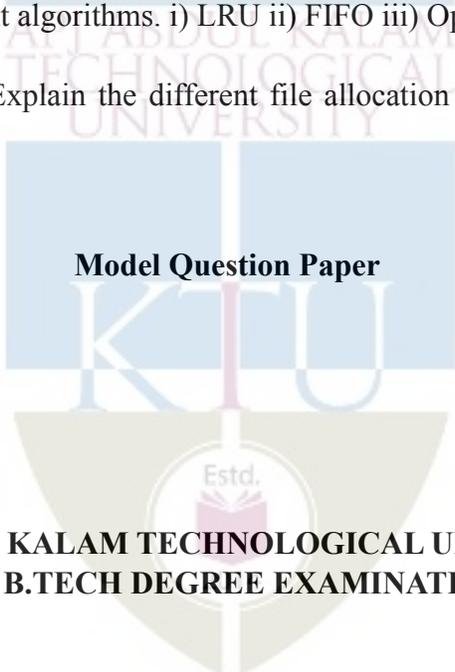
Model Question Paper

QP CODE: PAGES: ___

Reg No:_____
Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FOURTH SEMESTER B.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Code: CST 206

Course name : OPERATING SYSTEMS

Max Marks: 100   **Duration: 3 Hours**

PART-A

(Answer All Questions. Each question carries 3 marks)

1. How does hardware find the Operating System kernel after system switch-on?

2. What is the purpose of system call in operating system?

3. Why is context switching considered as an overhead to the system?

4. How is inter process communication implement using shared memory?

5. Describe resource allocation graph for the following.

    a) with a deadlock   b)with a cycle but no deadlock.

6. What is critical section? What requirement should be satisfied by a solution to the critical section problem?

7. Consider the reference string 1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 2, 3, 7, 6, 3, 2, 1, 2, 3, 6. How many page faults occur while using FCFS for the following cases.

    a) frame=2   b)frame=3

8. Differentiate between internal and external fragmentations.

9. Compare sequential access and direct access methods of storage devices.

10. Define the terms (i) Disk bandwidth (ii) Seek time.

PART-B(Answer any one question from each module)

11. a) Explain the following structures of operating system (i) Monolithic systems
         (ii) Layered Systems (iii) Micro Kernel (iv) Modular approach.   **(12)**

     b) Under what circumstances would a user be better of using a time sharing system than a PC or a single user workstation?   **(2)**

OR

12. a) What is the main advantage of the micro kernel approach to system design? How do user program and system program interact in a microkernel architecture?   **(8)**

    b) Describe the differences between symmetric and asymmetric multiprocessing? What are the advantages and disadvantages of multiprocessor systems?   **(6)**

13. a) Define process. With the help of a neat diagram explain different states of process.   **(8)**
    b) Explain how a new process can be created in Unix using fork system call.   **(6)**

OR

14 a) Find the average waiting time and average turnaround time for the processes given in the table below using:- i) SRT scheduling algorithm ii) Priority scheduling algorithm   **(9)**

Process	Arrival Time (ms)	CPU Burst Time (ms)	Priority
P1	0	5	3
P2	2	4	1
P3	3	1	2
P4	5	2	4

b) What is a Process Control Block? Explain the fields used in a Process Control Block. **(5)**

15. Consider a system with five processes P_0 through P_4 and three resources of type A, B, C. Resource type A has 10 instances, B has 5 instances and C has 7 instances. Suppose at time t_0 following snapshot of the system has been taken:

Process	Allocation			Max			Available		
	A	B	C	A	B	C	A	B	C
P_0	0	1	0	7	5	3	3	3	2
P_1	2	0	0	3	2	2			
P_2	3	0	2	9	0	2			
P_3	2	1	1	2	2	2			
P_4	0	0	2	4	3	3			

i) What will be the content of the Need matrix? Is the system in a safe state? If Yes, then what is the safe sequence?   **(8)**

iii) What will happen if process P_1 requests one additional instance of resource type A and two instances of resource type C?   **(6)**

OR

16. a) State dining philosopher's problem and give a solution using semaphores.   **(7)**

b) What do you mean by binary semaphore and counting semaphore? With C struct, explain implementation of wait () and signal()   **(7)**

17. a) Consider the following page reference string 1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 2, 3, 7, 6, 3, 2, 1, 2, 3, 6. Find out the number of page faults if there are 4 page frames, using the following page replacement algorithms i) LRU ii) FIFO iii) Optimal **(9)**

b) Explain the steps involved in handling a page fault. **(5)**

OR

18. a) With a diagram, explain how paging is done with TLB. **(5)**

b) Memory partitions of sizes 100 kb, 500 kb, 200 kb, 300 kb, 600 kb are available, how would best ,worst and first fit algorithms place processes of size 212 kb, 417 kb, 112 kb, 426 kb in order. Rank the algorithms in terms of how efficiently they uses memory. **(9)**

19. a) Suppose that a disk drive has 5000 cylinders, numbered 0 to 4999. the drive currently services a request at cylinder 143, and the previous request was at cylinder 125. the queue of pending request in FIFO order is 86, 1470, 913, 1774, 948, 1509, 1022, 1750, 130. Starting from the current position, what is the total distance (in cylinders) that the disk arm moves to satisfy all pending requests for each of the following algorithms

  i) FCFS   ii) SSFT   iii) SCAN   iv) LOOK   v) C-SCAN **(10)**

b) What is the use of access matrix in protection mechanism? **(4)**

OR

20. a) Explain the different file allocation operations with advantages and disadvantages. **(8)**
    b) Explain the following i) file types ii) file operation iii) file attributes **(6)**

Teaching Plan

	Module 1 - Introduction	**5 Hours**
1.1	Introduction to Operating System	1
1.2	Operating System operations, functions, service	1
1.3	System calls, Types	1
1.4	Operating System Structure: Simple, Layered, Microkernel, Modules	1
1.5	System Boot Process	1
	Module 2 – Processes and Process Scheduling	**9 Hours**
2.1	Processes, Process states	1
2.2	Process Control Block, Threads	1

2.3	Scheduling	1
2.4	Operations on processes: process creation and termination	1
2.5	Inter-process communication: Shared memory systems, Message Passing	1
2.6	Process Scheduling – Basic concepts, Scheduling Criteria	1
2.7	Scheduling algorithms - Basics	1
2.8	First come First Served, Shortest Job First	1
2.9	Priority scheduling, Round Robin Scheduling	1
	Module 3 - Process synchronization and Dead locks	**13 Hours**
3.1	Process synchronization, Race conditions	1
3.2	Critical Section problem, Peterson's solution	1
3.3	Synchronization hardware, Mutex Locks	1
3.4	Semaphores	1
3.5	Monitors	1
3.6	Synchronization problem examples (Lecture 1)	1
3.7	Synchronization problem examples (Lecture 2)	1
3.8	Deadlocks: Necessary conditions, Resource Allocation Graphs	1
3.9	Deadlock prevention	1
3.10	Deadlock avoidance	1
3.11	Banker's algorithm	1
3.12	Deadlock detection	1
3.13	Deadlock recovery	1
	Module 4 - Memory Management	**9 Hours**
4.1	Memory Management: Concept of Address spaces	1
4.2	Swapping	1
4.3	Contiguous memory allocation, fixed and variable partitions	1
4.4	Segmentation.	1
4.5	Paging (Lecture 1)	1
4.6	Paging (Lecture 2)	1
4.7	Virtual memory, Demand Paging	1

4.8	Page replacement algorithms (Lecture 1)	1
4.9	Page replacement algorithms (Lecture 2)	1
	Module 5 - File and Disk management	**9 Hours**
5.1	File concept, Attributes, Operations, types, structure	1
5.2	Access methods	1
5.3	Protection	1
5.4	File-System implementation	1
5.5	Directory implementation	1
5.6	Allocation methods	1
5.7	Magnetic disks, Solid-state disks, Disk structure	1
5.8	Disk scheduling	1
5.9	Disk formatting	1
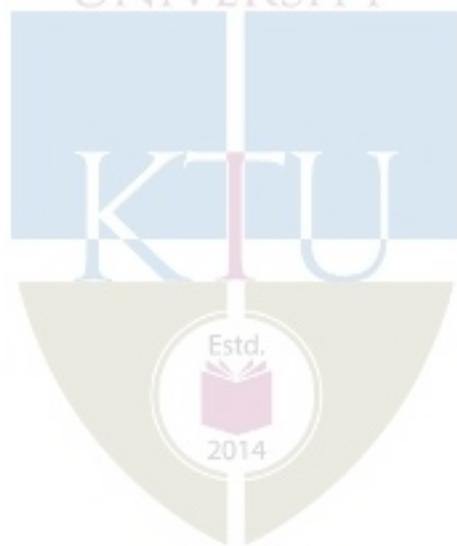
CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
			2	0	0	2
EST 200	DESIGN AND ENGINEERING					

Preamble:

The purpose of this course is to

     i) introduce the undergraduate engineering studentsthe fundamental principles of design engineering,

     ii) make them understand the steps involved in the design process and

     iii) familiarize them with the basic tools used and approaches in design.

Students are expected to apply design thinking in learning as well as while practicing engineering, which is very important and relevant for today. Case studies from various practical situations will help the students realize that design is not only concerned about the function but also many other factors like customer requirements, economics, reliability, etc. along with a variety of life cycle issues.

The course will help students to consider aesthetics, ergonomics and sustainability factors in designs and also to practice professional ethics while designing.

Prerequisite:

Nil. The course will be generic to all engineering disciplines and will not require specialized preparation or prerequisites in any of the individual engineering disciplines.

Course Outcomes:

After the completion of the course the student will be able to

CO 1	Explain the different concepts and principles involved in design engineering.
CO 2	Apply design thinking while learning and practicing engineering.
CO 3	Develop innovative, reliable, sustainable and economically viable designs incorporating knowledge in engineering.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	2	1					1			1		
CO 2		2				1		1				2
CO 3			2			1	1		2	2		1

Assessment Pattern

Continuous Internal Evaluation (CIE) Pattern:

Attendance	: 10 marks
Continuous Assessment Test (2 numbers)	: 25 marks
Assignment/Quiz/Course project	: 15 marks

End Semester Examination (ESE) Pattern: There will be two parts; Part A and Part B.

Part A	: 30 marks
part B	: 70 marks

Part A contains 10 questions with 2 questions from each module, having 3 marks for each question.
Students should answer all questions.
Part B contains 2 case study questions from each module of which student should answer any one.
Each question carry 14 marks and can have maximum 2 sub questions.

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	50	100	3 hours

Bloom's Category	Continuous Assessment Tests		End Semester Examination
	1	2	
Remember	5	5	10
Understand	10	10	20
Apply	35	35	70
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-

Course Level Assessment Questions

Course Outcome 1 (CO1): Appreciate the different concepts and principles involved in design engineering.

1. State how engineering design is different from other kinds of design

2. List the different stages in a design process.

3. Describedesign thinking.

4. State the function of prototyping and proofing in engineering design.

5. Write notes on the following concepts in connection with design engineering 1) Modular Design, 2) Life Cycle Design , 3) Value Engineering, 4) Concurrent Engineering, and 5) Reverse Engineering

6. State design rights.

Course Outcome 2 (CO2) Apply design thinking while learning and practicing engineering.

1. Construct the iterative process for design thinking in developing simple products like a pen, umbrella, bag, etc.

2. Show with an example how divergent-convergent thinking helps in generating alternative designs and then how to narrow down to the best design.

3. Describe how a problem-based learning helps in creating better design engineering solutions.

4. Discuss as an engineer, how ethics play a decisive role in your designs

Course Outcome 3(CO3): Develop innovative, reliable, sustainable and economically viable designs incorporating different segments of knowledge in engineering.

1. Illustratethe development of any simple product by passing through the different stages of design process

2. Show thegraphical design communication with the help of detailed 2D or 3D drawings for any simple product.

3. Describe how to develop new designs for simple products through bio-mimicry.

Model Question paper

Page 1 of 2

Reg No.:_____   Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD/FOURTH SEMESTER B.TECH DEGREE EXAMINATION

Course Code: EST 200

Course Name: DESIGN AND ENGINEERING

Max. Marks: 100Duration: 3 Hours

PART A

Answer all questions, each question carries 3 marks

Use only hand sketches

(1)Write aboutthe basic design process.

(2) Describe how to finalize the design objectives.

(3) State the role of divergent-convergent questioning in design thinking.

(4) Discuss how to perform design thinking in a team managing the conflicts.

(5) Show how engineering sketches and drawings convey designs.

(6)Explain the role of mathematics and physics in design engineering process.

(7) Distinguish between project-based learning and problem-based learning in design engineering.

(8) Describe how concepts like value engineering , concurrent engineering and reverse engineering influence engineering designs?

(9) Show how designs are varied based on the aspects of production methods, life span, reliability and environment?

(10) Explain how economics influence the engineering designs?

(10x3 marks =30 marks)

Part B

Answer any ONE question from each module. Each question carry 14 marks

Module 1

(11) Show the designing of a wrist watch going through the various stages of the design process. Use hand sketches to illustrate the processes.

or

(12)Find the customer requirements for designing a new car showroom. Show how the design objectives were finalized considering the design constraints?

Module 2

(13) Illustrate the design thinking approach for designing a bag for college students within a limited budget. Describe each stage of the process and the iterative procedure involved. Use hand sketches to support your arguments.

or

(14) Construct a number of possible designs and then refine them to narrow down to the best design for a drug trolley used in hospitals. Show how the divergent-convergent thinking helps in the process. Provide your rationale for each step by using hand sketches only.

Module 3

(15) Graphically communicate the design of a thermo flask used to keep hot coffee. Draw the detailed 2D drawings of the same with design detailing, material selection, scale drawings, dimensions, tolerances, etc. Use only hand sketches.

or

(16) Describe the role of mathematical modelling in design engineering. Show how mathematics and physics play a role in designing a lifting mechanism to raise 100 kg of weight to a floor at a height of 10 meters in a construction site.

Module 4

(17) Show the development of a nature inspired design for a solar poweredbus waiting shed beside a highway. Relate between natural and man-made designs. Use hand sketches to support your arguments.

or

(18) Show the design of a simple sofa and then depict how the design changes when considering 1) aesthetics and 2) ergonomics into consideration. Give hand sketches and explanations to justify the changes in designs.

Module 5

(19) Examine the changes in the design of a foot wear with constraints of 1) production methods, 2) life span requirement, 3) reliability issues and 4) environmental factors. Use hand sketches and give proper rationalization for the changes in design.

or

(20) Describe the how to estimate the cost of a particular design using ANY of the following: i) a website, ii) the layout of a plant, iii) the elevation of a building, iv) anelectrical or electronic system or device and v) a car.

Show how economics will influence the engineering designs. Use hand sketches to support your arguments.

(5x14 marks =70 marks)

Syllabus

Module 1

Design Process:- Introduction to Design and Engineering Design, Defining a Design Process-:Detailing Customer Requirements, Setting Design Objectives, Identifying Constraints, Establishing Functions, Generating Design Alternatives and Choosing a Design.

Module 2

Design Thinking Approach:-Introduction to Design Thinking, Iterative Design Thinking Process Stages: Empathize, Define, Ideate, Prototype and Test. Design Thinking as Divergent-Convergent Questioning. Design Thinking in a Team Environment.

Module 3

Design Communication (Languages of Engineering Design):-Communicating Designs Graphically, Communicating Designs Orally and in Writing. Mathematical Modeling In Design, Prototyping and Proofing the Design.

Module 4

Design Engineering Concepts:-Project-based Learning and Problem-based Learning in Design.Modular Design and Life Cycle Design Approaches. Application of Bio-mimicry,Aesthetics and Ergonomics in Design. Value Engineering, Concurrent Engineering, and Reverse Engineering in Design.

Module 5

Expediency, Economics and Environment in Design Engineering:-Design for Production, Use, and Sustainability. Engineering Economics in Design. Design Rights. Ethics in Design

Text Books

1) YousefHaik, SangarappillaiSivaloganathan, Tamer M. Shahin, Engineering Design Process, Cengage Learning 2003, Third Edition, ISBN-10: 9781305253285,

2) Voland, G., Engineering by Design, Pearson India 2014, Second Edition, ISBN 9332535051

Reference Books

1.Philip Kosky, Robert Balmer, William Keat, George Wise, Exploring Engineering, Fourth Edition: An Introduction to Engineering and Design, Academic Press 2015, 4th Edition, ISBN: 9780128012420.
2. Clive L. Dym, Engineering Design: A Project-Based Introduction, John Wiley & Sons, New York 2009, Fourth Edition, ISBN: 978-1-118-32458-5
3. Nigel Cross, Design Thinking: Understanding How Designers Think and Work, Berg Publishers 2011, First Edition, ISBN: 978-1847886361
4. Pahl, G., Beitz, W., Feldhusen, J., Grote, K.-H., Engineering Design: A Systematic Approach, Springer 2007, Third Edition, ISBN 978-1-84628-319-2

Course Contents and Lecture Schedule

No	Topic	No. of Lectures
1	**Module 1: Design Process**	
1.1	Introduction to Design and Engineering Design. *What does it mean to design something? How Is engineering design different from other kinds of design? Where and when do engineers design? What are the basic vocabularyin engineering design? How to learn and do engineering design.*	1
1.2	*Defining a Design Process*-: Detailing Customer Requirements. *How to do engineering design? Illustrate the process with an example. How to identify the customer requirements of design?*	1
1.3	*Defining a Design Process*-: Setting Design Objectives, Identifying Constraints, Establishing Functions. *How to finalize the design objectives? How to identify the design constraints? How to express the functions a design in engineering terms?*	1
1.4	*Defining a Design Process*-: Generating Design Alternatives and Choosing a Design. *How to generate or create feasible design alternatives? How to identify the "best possible design"?*	1
1.5	Case Studies:- Stages of Design Process. *Conduct exercises for designing simple products going through the different stages of design process.*	1
2	**Module 2: Design Thinking Approach**	
2.1	Introduction to Design Thinking *How does the design thinking approach help engineers in creating innovative and efficient designs?*	1
2.2	Iterative Design Thinking Process Stages: Empathize, Define, Ideate, Prototype and Test. *How can the engineers arrive at better designs utilizing the iterative design thinking process (in which knowledge acquired in the later stages can be applied back to the earlier stages)?*	1
2.3	Design Thinking as Divergent-Convergent Questioning. *Describe how to create a number of possible designs and then how to refine and narrow down to the 'best design'.*	1
2.4	Design Thinking in a Team Environment. *How to perform design thinking as a team managing the conflicts ?*	1
2.5	Case Studies: Design Thinking Approach. *Conduct exercises using the design thinking approach for*	1

	designing any simple products within a limited time and budget	
3	**Module 3: Design Communication (Languages of Engineering Design)**	
3.1	Communicating Designs Graphically. *How do engineering sketches and drawings convey designs?*	1
3.2	Communicating Designs Orally and in Writing. *How can a design be communicated through oral presentation or technical reports efficiently?*	1
	First Series Examination	
3.3	Mathematical Modelling in Design. *How do mathematics and physics become a part of the design process?*	1
3.4	Prototyping and Proofing the Design. *How to predict whether the design will function well or not?*	1
3.5	Case Studies: Communicating Designs Graphically. *Conduct exercises for design communication through detailed 2D or 3D drawings of simple products with design detailing, material selection, scale drawings, dimensions, tolerances, etc.*	1
4	**Module 4: Design Engineering Concepts**	
4.1	Project-based Learning and Problem-based Learning in Design. *How engineering students can learn design engineering through projects?* *How students can take up problems to learn design engineering?*	1
4.2	Modular Design and Life Cycle Design Approaches. *What is modular approach in design engineering? How it helps?* *How the life cycle design approach influences design decisions?*	1
4.3	Application of Bio-mimicry, Aesthetics and Ergonomics in Design. *How do aesthetics and ergonomics change engineering designs?* *How do the intelligence in nature inspire engineering designs? What are the common examples of bio-mimicry in engineering?*	1
4.4	Value Engineering, Concurrent Engineering, and Reverse Engineering in Design. *How do concepts like value engineering , concurrent engineering and reverse engineering influence engineering designs?*	1
4.5	Case Studies: Bio-mimicry based Designs. *Conduct exercises to develop new designs for simple*	1

	products using bio-mimicry and train students to bring out new nature inspired designs.	
5	**Module 5: Expediency, Economics and Environment in Design Engineering**	
5.1	Design for Production, Use, and Sustainability. *How designs are finalized based on the aspects of production methods, life span, reliability and environment?*	1
5.2	Engineering Economics in Design. *How to estimate the cost of a particular design and how will economics influence the engineering designs?*	1
5.3	Design Rights. *What are design rights and how can an engineer put it into practice?*	1
5.4	Ethics in Design. *How do ethics play a decisive role in engineering design?*	1
5.5	Case Studies: Design for Production, Use, and Sustainability. *Conduct exercises using simple products to show how designs change with constraints of production methods, life span requirement, reliability issues and environmental factors.*	1
Second Series Examination		

Code.	Course Name	L	T	P	Hrs	Credit
HUT 200	**Professional Ethics**	2	0	0	2	2

Preamble: To enable students to create awareness on ethics and human values.

Prerequisite: Nil

Course Outcomes: After the completion of the course the student will be able to

CO 1	Understand the core values that shape the ethical behaviour of a professional.
CO 2	Adopt a good character and follow an ethical life.
CO 3	Explain the role and responsibility in technological development by keeping personal ethics and legal ethics.
CO 4	Solve moral and ethical problems through exploration and assessment by established experiments.
CO 5	Apply the knowledge of human values and social values to contemporary ethical values and global issues.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12
CO 1								2			2	
CO 2								2			2	
CO 3								3			2	
CO 4								3			2	
CO 5								3			2	

Assessment Pattern

Bloom's category	Continuous Assessment Tests		End Semester Exam
	1	2	
Remember	15	15	30
Understood	20	20	40
Apply	15	15	30

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance	:	10 marks
Continuous Assessment Tests (2 Nos)	:	25 marks
Assignments/Quiz	:	15 marks

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contains 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

Course Level Assessment Questions

Course Outcome 1 (CO1):
1. Define integrity and point out ethical values.
2. Describe the qualities required to live a peaceful life.
3. Explain the role of engineers in modern society.

Course Outcome 2 (CO2)
1. Derive the codes of ethics.
2. Differentiate consensus and controversy.
3. Discuss in detail about character and confidence.

Course Outcome 3(CO3):
1. Explain the role of professional's ethics in technological development.
2. Distinguish between self interest and conflicts of interest.
3. Review on industrial standards and legal ethics.

Course Outcome 4 (CO4):
1. Illustrate the role of engineers as experimenters.
2. Interpret the terms safety and risk.
3. Show how the occupational crimes are resolved by keeping the rights of employees.

Course Outcome 5 (CO5):
1. Exemplify the engineers as managers.
2. Investigate the causes and effects of acid rain with a case study.
3. Explore the need of environmental ethics in technological development.

Model Question paper

QP CODE: Reg No:_____

PAGES:3   Name :_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY THIRD/FOURTH SEMESTER B.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Code: HUT 200
Course Name: PROFESSIONAL ETHICS

Max. Marks: 100   Duration: 3 Hours

(2019-Scheme)

PART A

(Answer all questions, each question carries 3 marks)

1. Define empathy and honesty.

2. Briefly explain about morals, values and ethics.

3. Interpret the two forms of self-respect.

4. List out the models of professional roles.

5. Indicate the advantages of using standards.

6. Point out the conditions required to define a valid consent?

7. Identify the conflicts of interests with an example?

8. Recall confidentiality.

9. Conclude the features of biometric ethics.

10. Name any three professional societies and their role relevant to engineers.

                                                              (10x3 = 30 marks)

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. **a)** Classify the relationship between ethical values and law?

    b) Compare between caring and sharing.   (10+4 = 14 marks)

Or

12. **a)** Exemplify a comprehensive review about integrity and respect for others.

b) Discuss about co-operation and commitment.   (8+6 = 14 marks)

MODULE II

13.a) Explain the three main levels of moral developments, deviced by Kohlberg.

b) Differentiate moral codes and optimal codes.   (10+4 = 14 marks)

Or

14. a) Extrapolate the duty ethics and right ethics.

b) Discuss in detail the three types of inquiries in engineering ethics   (8+6 = 14 marks)

MODULE III

15.a) Summarize the following features of morally responsible engineers.

(i) Moral autonomy   **(ii)** Accountability

b)Explain the rights of employees   (8+6 = 14 marks)

Or

16. a) Explain the reasons for Chernobyl mishap ?

b) Describe the methods to improve collegiality and loyalty.   (8+6 = 14 marks)

MODULE IV

17.a) Execute collegiality with respect to commitment, respect and connectedness.

b) Identify conflicts of interests with an example.   (8+6 = 14 marks)

Or

18. a) Explain in detail about professional rights and employee rights.

b) Exemplify engineers as managers.

MODULE V

19.a) Evaluate the technology transfer and appropriate technology.

b) Explain about computer and internet ethics.   (8+6 = 14 marks)

Or

20. a) Investigate the causes and effects of acid rain with a case study.

b) Conclude the features of ecocentric and biocentric ethics.   (8+6 = 14 marks)

Syllabus

Module 1 – Human Values.

Morals, values and Ethics – Integrity- Academic integrity-Work Ethics- Service Learning- Civic Virtue-Respect for others- Living peacefully- Caring and Sharing- Honestly- courage-Cooperation commitment-Empathy-Self Confidence -Social Expectations.

Module 2 - Engineering Ethics & Professionalism.

Senses of Engineering Ethics - Variety of moral issues- Types of inquiry- Moral dilemmas –Moral Autonomy – Kohlberg's theory- Gilligan's theory- Consensus and Controversy-Profession and Professionalism- Models of professional roles-Theories about right action –Self interest-Customs and Religion- Uses of Ethical Theories.

Module 3- Engineering as social Experimentation.

Engineering as Experimentation – Engineers as responsible Experimenters- Codes of Ethics- Plagiarism-A balanced outlook on law - Challenges case study- Bhopal gas tragedy.

Module 4- Responsibilities and Rights.

Collegiality and loyalty – Managing conflict- Respect for authority- Collective bargaining- Confidentiality-Role of confidentiality in moral integrity-Conflicts of interest- Occupational crime- Professional rights-Employee right- IPR Discrimination.

Module 5- Global Ethical Issues.

Multinational Corporations- Environmental Ethics- Business Ethics- Computer Ethics -Role in Technological Development-Engineers as Managers- Consulting Engineers- Engineers as Expert witnesses and advisors-Moral leadership.

Text Book

1. M Govindarajan, S Natarajan and V S Senthil Kumar, Engineering Ethics, PHI Learning Private Ltd, New Delhi,2012.

2. R S Naagarazan, A text book on professional ethics and human values, New age international (P) limited ,New Delhi,2006.

Reference Books

1. Mike W Martin and Roland Schinzinger, Ethics in Engineering,4th edition, Tata McGraw Hill Publishing Company Pvt Ltd, New Delhi,2014.
2. Charles D Fleddermann, Engineering Ethics, Pearson Education/ Prentice Hall of India, New Jersey,2004.
3. Charles E Harris, Michael S Protchard and Michael J Rabins, Engineering Ethics- Concepts and cases, Wadsworth Thompson Learning, United states,2005.
4. http://www.slideword.org/slidestag.aspx/human-values-and-Professional-ethics**.**

Course Contents and Lecture Schedule

SL.No	Topic	No. of Lectures 25
1	**Module 1 – Human Values.**	
1.1	Morals, values and Ethics, Integrity, Academic Integrity,Work Ethics	1
1.2	Service Learning, Civic Virtue, Respect for others, Living peacefully	1
1.3	Caring and Sharing, Honesty, Courage, Co-operation commitment	2
1.4	Empathy, Self Confidence, Social Expectations	1
2	**Module 2- Engineering Ethics & Professionalism.**	
2.1	Senses of Engineering Ethics, Variety of moral issues, Types of inquiry	1
2.2	Moral dilemmas, Moral Autonomy, Kohlberg's theory	1
2.3	Gilligan's theory, Consensus and Controversy,Profession& Professionalism, Models of professional roles, Theories about right action	2
2.4	Self interest-Customs and Religion, Uses of Ethical Theories	1
3	**Module 3- Engineering as social Experimentation.**	
3.1	Engineering as Experimentation, Engineers as responsible Experimenters	1
3.2	Codes of Ethics,Plagiarism, A balanced outlook on law	2
3.3	Challenger case study, Bhopal gas tragedy	2
4	**Module 4- Responsibilities and Rights.**	
4.1	Collegiality and loyalty, Managing conflict, Respect for authority	1
4.2	Collective bargaining, Confidentiality, Role of confidentiality in moral integrity, Conflicts of interest	2
4.3	Occupational crime, Professional rights, Employee right, IPR Discrimination	2
5	**Module 5- Global Ethical Issues.**	
5.1	Multinational Corporations, Environmental Ethics, Business Ethics, Computer Ethics	2
5.2	Role in Technological Development, Moral leadership	1
5.3	Engineers as Managers, Consulting Engineers, Engineers as Expert witnesses and advisors	2

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
MCN202	CONSTITUTION OF INDIA		2	0	0	NIL

Preamble:

The study of their own country constitution and studying the importance environment as well as understanding their own human rights help the students to concentrate on their day to day discipline. It also gives the knowledge and strength to face the society and people.

Prerequisite: Nil

Course Outcomes: After the completion of the course the student will be able to

CO 1	Explain the background of the present constitution of India and features.
CO 2	Utilize the fundamental rights and duties.
CO 3	Understand the working of the union executive, parliament and judiciary.
CO 4	Understand the working of the state executive, legislature and judiciary.
CO 5	Utilize the special provisions and statutory institutions.
CO 6	Show national and patriotic spirit as responsible citizens of the country

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1						2	2	2		2		
CO 2						3	3	3		3		
CO 3						3	2	3		3		
CO 4						3	2	3		3		
CO 5						3	2	3		3		
CO 6						3	3	3		2		

Assessment Pattern

Bloom's Category	Continuous Assessment Tests		End Semester Examination
	1	2	
Remember	20	20	40
Understand	20	20	40
Apply	10	10	20
Analyse			

Evaluate			
Create			

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance   : 10 marks
Continuous Assessment Test (2 numbers)   : 25 marks
Assignment/Quiz/Course project   : 15 marks

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

Course Level Assessment Questions

Course Outcome 1 (CO1):

1 Discuss the historical background of the Indian constitution.

2 Explain the salient features of the Indian constitution.

3 Discuss the importance of preamble in the implementation of constitution.

Course Outcome 2 (CO2)

1 What are fundamental rights ? Examine each of them.

2 Examine the scope of freedom of speech and expression underlying the constitution.

3 The thumb impression of an accused is taken by the police against his will. He contends

   that this is a violation of his rights under Art 20(3) of the constitution. Decide.

Course Outcome 3(CO3):

1 Explain the powers of the President to suspend the fundamental rights during emergency.

2 Explain the salient features of appeal by special leave.

3. List the constitutional powers of President.

Course Outcome 4 (CO4):

1 Discuss the constitutional powers of Governor.

2 Examine the writ jurisdiction of High court.

3 Discuss the qualification and disqualification of membership of state legislature.

Course Outcome 5 (CO5):

1 Discuss the duties and powers of comptroller of auditor general.

2 Discuss the proclamation of emergency.

3 A state levies tax on motor vehicles used in the state, for the purpose of maintaining roads

in the state. X challenges the levy of the tax on the ground that it violates the freedom of

interstate commerce guaranteed under Art 301. Decide.

Course Outcome 6 (CO6):

1 Explain the advantages of citizenship.

2 List the important principles contained in the directive principles of state policy.

3 Discuss the various aspects contained in the preamble of the constitution

Model Question paper

PART A

(Answer all questions. Each question carries 3 marks)

1 Define and explain the term constitution.

2 Explain the need and importance of Preamble.

3 What is directive principle of state policy?

4 Define the State.

5 List the functions of Attorney general of India.

6 Explain the review power of Supreme court.

7 List the qualifications of Governor.

8 Explain the term and removal of Judges in High court.

9 Explain the powers of public service commission.

10 List three types of emergency under Indian constitution.

(10X3=30marks)

PART B

(Answer on question from each module. Each question carries 14 marks)

Module 1

11 Discuss the various methods of acquiring Indian citizenship.

12 Examine the salient features of the Indian constitution.

Module 2

13 A high court passes a judgement against X. X desires to file a writ petition in the supreme

court under Art32, on the ground that the judgement violates his fundamental rights.

Advise him whether he can do so.

14 What is meant by directive principles of State policy? List the directives.

Module3

15 Describe the procedure of election and removal of the President of India.

16 Supreme court may in its discretion grant special leave to appeal. Examine the situation.

Module 4

17 Discuss the powers of Governor.

18 X filed a writ petition under Art 226 which was dismissed. Subsequently, he filed a writ

petition under Art 32 of the constitution, seeking the same remedy. The Government

argued that the writ petition should be dismissed, on the ground of res judicata. Decide.

Module 5

19 Examine the scope of the financial relations between the union and the states.

20 Discuss the effects of proclamation of emergency.

(14X5=70marks)

Syllabus

Module 1 Definition, historical back ground, features, preamble, territory, citizenship.

Module 2 State, fundamental rights, directive principles, duties.

Module 3 The machinery of the union government.

Module 4 Government machinery in the states

Module 5 The federal system, Statutory Institutions, miscellaneous provisions.

Text Books

1 D D Basu, Introduction to the constitution of India, Lexis Nexis, New Delhi, 24e, 2019

2 PM Bhakshi, The constitution of India, Universal Law, 14e, 2017

Reference Books

1 Ministry of law and justice, The constitution of India, Govt of India, New Delhi, 2019.

2 JN Pandey, The constitutional law of India, Central Law agency, Allahabad, 51e, 2019

3 MV Pylee, India's Constitution, S Chand and company, New Delhi, 16e, 2016

Course Contents and Lecture Schedule

No	Topic	No. of Lectures
1	**Module 1**	
1.1	Definition of constitution, historical back ground, salient features of the constitution.	1
1.2	Preamble of the constitution, union and its territory.	1
1.3	Meaning of citizenship, types, termination of citizenship.	2
2	**Module 2**	
2.1	Definition of state, fundamental rights, general nature, classification, right to equality ,right to freedom , right against exploitation	2

2.2	Right to freedom of religion, cultural and educational rights, right to constitutional remedies. Protection in respect of conviction for offences.	2
2.3	Directive principles of state policy, classification of directives, fundamental duties.	2
3	**Module 3**	
3.1	The Union executive, the President, the vice President, the council of ministers, the Prime minister, Attorney-General, functions.	2
3.2	The parliament, composition, Rajya sabha, Lok sabha, qualification and disqualification of membership, functions of parliament.	2
3.3	Union judiciary, the supreme court, jurisdiction, appeal by special leave.	1
4	**Module 4**	
4.1	The State executive, the Governor, the council of ministers, the Chief minister, advocate general, union Territories.	2
4.2	The State Legislature, composition, qualification and disqualification of membership, functions.	2
4.3	The state judiciary, the high court, jurisdiction, writs jurisdiction.	1
5	**Module 5**	
5.1	Relations between the Union and the States, legislative relation, administrative relation, financial Relations, Inter State council, finance commission.	1
5.2	Emergency provision, freedom of trade commerce and inter course, comptroller and auditor general of India, public Services, public service commission, administrative Tribunals.	2
5.3	Official language, elections, special provisions relating to certain classes, amendment of the Constitution.	2

CSL 202	DIGITAL LAB	CATEGORY	L	T	P	CREDIT
		PCC	0	0	3	2

Preamble: This course helps the learners to get familiarized with (i) Digital Logic Design through the implementation of Logic Circuits using ICs of basic logic gates & flip-flops and (ii) Hardware Description Language based Digital Design. This course helps the learners to design and implement hardware systems in areas such as games, music, digital filters, wireless communications and graphical displays.

Prerequisite: Topics covered under the course Logic System Design **(CST 203)**

Course Outcomes: After the completion of the course the student will be able to

CO 1	Design and implement combinational logic circuits using Logic Gates (Cognitive Knowledge Level: **Apply**)
CO 2	Design and implement sequential logic circuits using Integrated Circuits (Cognitive Knowledge Level: **Apply**)
CO 3	Simulate functioning of digital circuits using programs written in a Hardware Description Language (Cognitive Knowledge Level: **Apply**)
CO 4	Function effectively as an individual and in a team to accomplish a given task of designing and implementing digital circuits (Cognitive Knowledge Level: **Apply**)

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12
CO 1	✔	✔	✔	✔				✔				✔
CO 2	✔	✔	✔	✔				✔				✔
CO 3	✔	✔	✔	✔	✔			✔				✔
CO 4	✔	✔	✔	✔				✔	✔			✔

Assessment Pattern

Bloom's Category	Continuous Assessment Test (Internal Exam) (Percentage)	End Semester Examination (Percentage)
Remember	20	20
Understand	20	20
Apply	60	60
Analyse		
Evaluate		
Create		

Mark Distribution

Total Marks	CIE Marks	ESE Marks	ESE Duration
150	75	75	3 hours

Continuous Internal Evaluation Pattern:

Attendance   : 15 marks

Continuous Evaluation in Lab   : 30 marks

Continuous Assessment Test   : 15 marks

Viva-voce   : 15 marks

Internal Examination Pattern: The marks will be distributed as Design/Algorithm 30 marks, Implementation/Program 20 marks, Output 20 marks and Viva 30 marks. Total 100 marks which will be converted out of 15 while calculating Internal Evaluation marks.

End Semester Examination Pattern: The marks will be distributed as Design/Algorithm 30 marks, Implementation/Program 20 marks, Output 20 marks and Viva 30 marks. Total 100 marks will be converted out of 75 for End Semester Examination.

Fair Lab Record:

All Students attending the Digital Lab should have a Fair Record. The fair record should be produced in the University Lab Examination. Every experiment conducted in the lab should be noted in the fair record. For every experiment in the fair record, the right hand page should contain Experiment Heading, Experiment Number, Date of Experiment, and Aim of Experiment. The left hand page should contain components used, circuit design or a print out of the code used for the experiment and sample output obtained.

SYLLABUS

Conduct a minimum of **8** experiments from **Part A** and a minimum of **4** experiments from **Part B**. The starred experiments in Part A are mandatory. The lab work should be conducted in groups (maximum group size being 4). The performance of a student in the group should be assessed based on teamwork, integrity and cooperation.

Part A (Any 8 Experiments)

- A 2 hour session should be spent to make the students comfortable with the use of trainer kit/breadboard and ICs.
- The following experiments can be conducted on breadboard or trainer kits.
- Out of the 15 experiments listed below, a minimum of 8 experiments should be completed by a student, including the mandatory experiments (5).

1. Realization of functions using basic and universal gates (SOP and POS forms).
2. Design and realization of half adder, full adder, half subtractor and full subtractor using: a) basic gates (b) universal gates. *
3. Code converters: Design and implement BCD to Excess 3 and Binary to Gray code converters.
4. Design and implement 4 bit adder/subtractor circuit and BCD adder using IC7483.
5. Implementation of Flip Flops: SR, D, T, JK and Master Slave JK Flip Flops using basic gates.*
6. Asynchronous Counter: Design and implement 3 bit up/down counter.
7. Asynchronous Counter: Realization of Mod N counters (At least one up counter and one down counter to be implemented). *
8. Synchronous Counter: Realization of 4-bit up/down counter.
9. Synchronous Counter: Realization of Mod-N counters and sequence generators. (At least one mod N counter and one sequence generator to be implemented) *
10. Realization of Shift Register (Serial input left/right shift register), Ring counter and Johnson Counter using flipflops. *
11. Realization of counters using IC's (7490, 7492, 7493).
12. Design and implement BCD to Seven Segment Decoder.
13. Realization of Multiplexers and De-multiplexers using gates.
14. Realization of combinational circuits using MUX & DEMUX ICs (74150, 74154).
15. To design and set up a 2-bit magnitude comparator using basic gates.

PART B (Any 4 Experiments)

- The following experiments aim at training the students in digital circuit design with *Verilog*. The experiments will lay a foundation for digital design with Hardware Description Languages.
- A 3 hour introductory session shall be spent to make the students aware of the fundamentals of development using Verilog
- Out of the 8 experiments listed below, a minimum of 4 experiments should be completed by a student

Experiment 1. Realization of Logic Gates and Familiarization of Verilog
(a) Familiarization of the basic syntax of Verilog
(b) Development of Verilog modules for basic gates and to verify truth tables.
(c) Design and simulate the HDL code to realize three and four variable Boolean functions

Experiment 2: Half adder and full adder
(a) Development of Verilog modules for half adder in 3 modeling styles (dataflow/ structural/behavioural).
(b) Development of Verilog modules for full adder in structural modeling using half adder.

Experiment 3: Design of code converters

Design and simulate the HDL code for

(a) 4- bit binary to gray code converter
(b) 4- bit gray to binary code converter

Experiment 4: Mux and Demux in Verilog
(a) Development of Verilog modules for a 4x1 MUX.
(b) Development of Verilog modules for a 1x4 DEMUX.

Experiment 5: Adder/Subtractor
(a) Write the Verilog modules for a 4-bit adder/subtractor
(b) Development of Verilog modules for a BCD adder

Experiment 6: Magnitude Comparator

Development of Verilog modules for a 4 bit magnitude comparator

Experiment 7: Flipflops and shiftregisters
(a) Development of Verilog modules for SR, JK, T and D flip flops.
(b) Development of Verilog modules for a Johnson/Ring counter

Experiment 8: Counters
(a) Development of Verilog modules for an asynchronous decade counter.
(b) Development of Verilog modules for a 3 bit synchronous up-down counter.

Practice Questions

PART A

1. Design a two bit parallel adder using gates and implement it using ICs of basic gates
2. A combinatorial circuit has 4 inputs and one output. The output is equal to 1 when (a) all inputs are 1, (b) none of the inputs are 1, (c) an odd number of inputs are equal to 1. Obtain the truth table and output function for this circuit and implement the same.
3. Design and implement a parallel subtractor.
4. Design and implement a digital circuit that converts Gray code to Binary.
5. Design a combinational logic circuit that will output the 1's compliment of a 4-bit input number.
6. Implement and test the logic function $f(A, B, C) = \sum m(0,1,3,6)$ using an 8:1 MUX IC
7. Design a circuit that will work as a ring counter or a Johnson counter based on a mode bit, M.
8. Design a 4-bit synchronous down counter.
9. Design a Counter to generate the binary sequence 0,1,3,7,6,4
10. Design an asynchronous mod 10 down counter
11. Design and implement a synchronous counter using JK flip flop ICs to generate the sequence: 0 - 1 -3 - 5 - 7 - 0.

PART B

1. Develop Verilog modules for a full subtractor in structural modeling using half subtractors.
2. Design a 4 bit parallel adder using Verilog.
3. Develop Verilog modules for a 4 bit synchronous down counter.
4. Write Verilog code for implementing a 8:1 multiplexer.
5. Develop Verilog modules for a circuit that converts Excess 3 code to binary.
6. Write the Verilog code for a JK Flip flop, and its test-bench. Use all possible combinations of inputs to test its working
7. Write the hardware description in Verilog of a 8-bit register with shift left and shift right modes of operations and test its functioning.
8. Write the hardware description in Verilog of a mod-N (N > 9) counter and test it.

CST 206	OPERATING SYSTEMS LAB	CATEGORY	L	T	P	CREDIT	YEAR OF INTRODUCTION
		PCC	0	0	3	2	2019

Preamble: The course aims to offer students a hands-on experience on Operating System concepts using a constructivist approach and problem-oriented learning. Operating systems are the fundamental part of every computing device to run any type of software.

Prerequisite: Topics covered in the courses are **Data Structures (CST 201)** and **Programming in C (EST 102)**

Course Outcomes:

At the end of the course, the student should be able to

CO1	Illustrate the use of systems calls in Operating Systems. **(Cognitive knowledge: Understand)**
CO2	Implement Process Creation and Inter Process Communication in Operating Systems. **(Cognitive knowledge: Apply)**
CO3	Implement Fist Come First Served, Shortest Job First, Round Robin and Priority-based CPU Scheduling Algorithms. **(Cognitive knowledge: Apply)**
CO4	Illustrate the performance of First In First Out, Least Recently Used and Least Frequently Used Page Replacement Algorithms. **(Cognitive knowledge: Apply)**
CO5	Implement modules for Deadlock Detection and Deadlock Avoidance in Operating Systems. **(Cognitive knowledge: Apply)**
CO6	Implement modules for Storage Management and Disk Scheduling in Operating Systems. **(Cognitive knowledge: Apply)**

Mapping of course outcomes with program outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓	✓	✓					✓		✓		✓
CO2	✓	✓	✓					✓		✓		✓
CO3	✓	✓	✓	✓				✓		✓		✓
CO4	✓	✓	✓	✓				✓		✓		✓
CO5	✓	✓	✓	✓				✓		✓		✓
CO6	✓	✓	✓	✓				✓		✓		✓

Abstract POs defined by National Board of Accreditation			
PO#	**Broad PO**	**PO#**	**Broad PO**
PO1	Engineering Knowledge	PO7	Environment and Sustainability
PO2	Problem Analysis	PO8	Ethics
PO3	Design/Development of solutions	PO9	Individual and team work
PO4	Conduct investigations of complex problems	PO10	Communication
PO5	Modern tool usage	PO11	Project Management and Finance
PO6	The Engineer and Society	PO12	Life long learning

Assessment Pattern:

Bloom's Category	Continuous Assessment Test (Internal Exam) Marks in percentage	End Semester Examination Marks in percentage
Remember	20	20
Understand	20	20
Apply	60	60
Analyse		
Evaluate		
Create		

Mark Distribution

Total Marks	CIE Marks	ESE Marks	ESE Duration
150	75	75	3 hours

Continuous Internal Evaluation Pattern:

Attendance	:	15 marks
Continuous Evaluation in Lab	:	30 marks
Continuous Assessment Test	:	15 marks
Viva Voce	:	15 marks

Internal Examination Pattern: The marks will be distributed as Algorithm 30 marks, Program 20 marks, Output 20 marks and Viva 30 marks. Total 100 marks which will be converted out of 15 while calculating Internal Evaluation marks.

End Semester Examination Pattern: The percentage of marks will be distributed as Algorithm 30 marks, Program 20 marks, Output 20 marks and Viva 30 marks. Total 75 marks.

Operating System to Use in Lab : **Linux**

Compiler/Software to Use in Lab : **gcc**

Progamming Language to Use in Lab : **Ansi C**

Fair Lab Record:

All Students attending the Operating System Lab should have a Fair Record. The fair record should be produced in the University Lab Examination. Every experiment conducted in the lab should be noted in the fair record. For every experiment in the fair record, the right hand page should contain Experiment Heading, Experiment Number, Date of experiment, Aim of the Experiment and the operations performed on them, Details of experiment including algorithm and result of Experiment. The left hand page should contain a print out of the code used for experiment and sample output obtained for a set of input.

SYLLABUS

OPERATING SYSTEMS LAB

* mandatory

1. Basic Linux commands
2. Shell programming

    -Command syntax

    -Write simple functions with basic tests, loops, patterns

3. System calls of Linux operating system:*

    fork, exec, getpid, exit, wait, close, stat, opendir, readdir

4. Write programs using the I/O system calls of Linux operating system (open, read, write)
5. Implement programs for Inter Process Communication using Shared Memory *
6. Implement Semaphores*
7. Implementation of CPU scheduling algorithms. a) Round Robin b) SJF c) FCFS d) Priority *
8. Implementation of the Memory Allocation Methods for fixed partition*

    a) First Fit b) Worst Fit c) Best Fit

9. Implement l page replacement algorithms a) FIFO b) LRU c) LFU*
10. Implement the banker's algorithm for deadlock avoidance. *
11. Implementation of Deadlock detection algorithm
12. Simulate file allocation strategies.

    b) Sequential b) Indexed c) Linked

13. Simulate disk scheduling algorithms. *

    c) FCFS b)SCAN c) C-SCAN

OPERATING SYSTEMS LAB - PRACTICE QUESTIONS

1. Write a program to create a process in linux.
2. Write programs using the following system calls of Linux operating system:

    fork, exec, getpid, exit, wait, close, stat, opendir, readdir

3. Write programs using the I/O system calls of Linux operating system (open, read, write)

4. Given the list of processes, their CPU burst times and arrival times, display/print the Gantt chart for FCFS and SJF. For each of the scheduling policies, compute and print the average waiting time and average turnaround time

5. Write a C program to simulate following non-preemptive CPU scheduling algorithms to find turnaround time and waiting time.

   a)FCFS b) SJF c) Round Robin (pre-emptive)   d) Priority

6. Write a C program to simulate following contiguous memory allocation techniques

   a) Worst-fit   b) Best-fit   c) First-fit

7. Write a C program to simulate paging technique of memory management.

8. Write a C program to simulate Bankers algorithm for the purpose of deadlock avoidance.

9. Write a C program to simulate disk scheduling algorithms a) FCFS b) SCAN c) C-SCAN

10. Write a C program to simulate page replacement algorithms a) FIFO b) LRU c) LFU

11. Write a C program to simulate producer-consumer problem using semaphores.

12. Write a program for file manipulation for display a file and directory in memory.

13. Write a program to simulate algorithm for deadlock prevention.

14. Write a C program to simulate following file allocation strategies.

   a)Sequential   b) Indexed   c) Linked